An Improved Monolithic Voltage-Controlled Amplifier

4055 (C-5)

Gary K. Hebert
THAT Corporation
Marlborough, MA 01752, USA

Presented at the 99th Convention 1995 October 6–9 New York

AES

AN AUDIO ENGINEERING SOCIETY PREPRINT

An Improved Monolithic Voltage-Controlled Amplifier

GARY K. HEBERT, *AES Member*

THAT Corporation, Marlborough, Massachusetts, USA

The design and implementation of a monolithic voltage-controlled amplifier with an exponential gain-control characteristic is described. Sources of deviation from ideal performance, including distortion, noise, offset change with gain, and noise modulation, are analyzed. Techniques used in this design to minimize these sources of error are described. Other factors influencing performance, such as stability, device geometry, physical layout, and the semiconductor process utilized, are discussed. Performance data on the resulting device is presented.

0 INTRODUCTION

Voltage-controlled amplifiers (VCAs) are devices which enable circuit gain to be controlled by an applied control voltage. Such devices are widely used in the professional audio industry as building blocks to implement such functions as remote gain-control, automated mixing, "dynamics processing" (compression, noise gating, de-essing, etc.), and voltage-controlled filtering. The type most widely used in such applications is that which exhibits an exponential gain-control characteristic over a wide range of gain and attenuation. In such devices a linear change in voltage at the control terminals gives rise to an exponential change in amplifier gain. This results in "dB-per-volt" control over gain that is particularly useful in audio applications.

This paper describes the design and implementation of a monolithic integrated circuit (IC) VCA which exhibits improved performance over previous designs. The first section describes reasons for the choice of the circuit topology used to implement the device. Subsequent sections identify the major sources of error in such devices and describes the approaches used in the current design to minimize these sources of error. Finally, performance data on the completed design is given to demonstrate the effectiveness of these efforts.

1 VCA TOPOLOGY

The majority of the topologies known to the author for implementing exponentially-controlled VCAs with professional-audio performance characteristics are based on the logarithmic relationship between the base-emitter voltage and collector current of the bipolar transistor, and are often referred to as "log-antilog VCAs". The principle of operation is illustrated by Figure 1. Referring to the figure, we may write by inspection, for positive V_{in}:

$$I_{in} = \frac{V_{in}}{R_{in}} \tag{1}$$

$$I_{out} = \frac{V_{out}}{R_{out}} \tag{2}$$

$$V_{be_1} = V_T \ln\left(\frac{I_{in}}{I_{S1}}\right) \tag{3}$$

$$V_{be2} = V_T \ln\left(\frac{I_{out}}{I_{S2}}\right) \tag{4}$$

$$V_c = V_{be2} - V_{be1} = V_T \ln\left(\frac{I_{out} I_{S1}}{I_{in} I_{S2}}\right) \tag{5}$$

$$\frac{I_{out}}{I_{in}} = \frac{I_{S2}}{I_{S1}} \exp\left(\frac{V_c}{V_T}\right) \tag{6}$$

Where V_T is the "thermal voltage", $\frac{kT}{q}$, and I_{S1} and I_{S2} are the saturation currents of Q1 and Q2 respectively. Assuming that Q1 and Q2 are matched devices and are at the same temperature, such that $I_{S1} = I_{S2}$, and that $R_{in} = R_{out}$, Equation (6) becomes:

$$\frac{V_{out}}{V_{in}} = \exp\left(\frac{V_c}{V_T}\right) \tag{7}$$

Thus, the circuit gain is exponentially controlled by the voltage V_c. (Though V_c is shown throughout this paper as a purely differential voltage, in practice typically either one or the other terminals is grounded, or V_c is driven differentially with a 0 volt common-mode voltage. This is necessary to avoid forward biasing any of the collector-base junctions of the core transistors.) Of course, the circuit in Figure 1 will only accept positive inputs for proper operation. Adding a sufficient DC bias to an incoming audio signal so that the input always met this condition would lead to an output offset that would be modulated by any changes in gain. So, alternatives have been designed to allow bipolar signals to be handled by a log-antilog VCA.

The techniques utilized to extend this approach to bipolar operation may be generally divided into two broad classes: those that utilize pairs of like-polarity devices exclusively to implement the log-antilog function, and those that utilize complementary pairs of devices. Examples of those in the first category are described in [1], [2], and [3]. Examples of those in the second category are described in [4], [5], [6], [7], and [8].

Utilizing all like-polarity, particularly all NPN, transistors for the logging and antilogging transistors (hereafter referred to as the core transistors) has an obvious advantage. High-performance, well-matched NPN devices are easily fabricated in standard junction-isolated bipolar IC processes. However, examination of references [1], [2], and [3] indicates that there are some disadvantages as well. Figure 2 shows conceptually an all NPN log-antilog VCA. Q1 and Q2, along with OA1 and OA2 function much like their counterparts in Figure 1, except that a bias current, I_{BIAS}, has been added to the emitters of Q1 and Q2. An additional, identical pair of log-antilog transistors, Q3 and Q4, has been added. These are driven with the same bias current and an inverted version of the signal from OA1. The collector current of Q3 is inverted by current mirror CM1 and summed with the collector current of Q2 to create the output current. The common bias current portions of these collector currents cancel, while the signal current

portions add. Similarly, the collector current of Q4 is inverted by current mirror CM2 and summed with the collector current of Q1 to create the feedback current returned to the inverting input of OA1.

The addition of the circuitry to create an inverted replica signal to drive Q3 and Q4, along with the current mirrors required to reinvert the signals at their collectors increases the die area required to implement the circuit. Of course, this tends to increase its cost. Further, the inverter following OA1 and current mirror CM2 lie inside the feedback loop around OA1. In high-performance designs such as those in [1], [2], and [3] the circuitry used to implement these functions can be rather complex. The additional circuitry inevitably adds high frequency poles to the loop transmission, complicating the frequency compensation of the loop and/or decreasing the gain-bandwidth product of the design. In fact, reference [2] details a variable compensation scheme wherein additional circuitry is employed to vary the loop compensation as a function of the VCA gain setting in order to combat this problem.

Figure 3 shows the simplest implementation of the complementary log-antilog VCA invented by David Blackmer in 1971 [4], and often referred to as the "Blackmer Gain Cell". In this circuit Q1, Q2, OA1, and OA2 again function similarly to their counterparts in Figure 1. PNP transistors Q3 and Q4 perform a similar log-antilog function for negative input signals. DC voltage source V_{BIAS} establishes dc bias currents through Q3-Q1 and Q4-Q2. This approach yields a relatively simple signal path. For low distortion performance, all four "core transistors," including the PNPs (Q3 and Q4), must be wide bandwidth, high current-gain devices, something not readily available in traditional junction-isolated bipolar IC processes. However, in recent years more advanced processes featuring high-performance vertical PNP transistors have become much more commonly available.

References [5], [6], [7], and [8] describe refinements of the complementary log-antilog VCA aimed at minimizing errors caused by non-ideal behavior of the core transistors. In particular, parasitic resistances in the bases and the emitters of these devices cause the collector current versus base-emitter voltage function to deviate from the ideal logarithmic behavior described in equations (3) and (4). The circuit shown in Figure 4 is described in reference [8]. This topology provides a means of minimizing errors due to parasitic resistances in the core transistors, along with other benefits, while retaining most of the simplicity of the original Blackmer gain cell. It is the topology chosen for the current design, and its operation is described in more detail in the following sections.

2 SOURCES OF DISTORTION

The major sources of distortion in log-antilog VCAs are parasitic base and emitter resistances in the core transistors, mismatches among the core transistors, and non-linearity in the input amplifier used to drive the core transistors. Each of these error sources is examined in the following sections, and the techniques used in the current design to minimize distortion from these sources are described.

2.1 Parasitic Resistances

Figure 5a shows parasitic resistances in series with each of the three terminals of the bipolar transistor. These are produced by the finite resistance of the silicon between the metallic contacts to the device and active base region underneath the emitter [9]. These resistances modify the ideal V_{be} versus I_c equation used in (3) and (4) as follows:

$$V_{be} = I_b r_b + I_e r_{ex} + V_T \ln\left(\frac{I_c}{I_S}\right). \tag{8}$$

(Note that the bulk emitter resistance is here denoted as r_{ex} rather than r_e to avoid confusion with the small signal emitter impedance $r_e = \frac{V_T}{I_C}$).

Remembering that $I_b = \frac{I_e}{\beta_F + 1}$, where β_F is the transistor's forward current gain, we may write:

$$V_{be} = I_e\left(r_{ex} + \frac{r_b}{\beta_F + 1}\right) + V_T \ln\left(\frac{I_c}{I_S}\right) = I_e r'_{ex} + V_T \ln\left(\frac{I_c}{I_S}\right), \tag{9}$$

where $r'_{ex} = r_{ex} + \frac{r_b}{\beta_F + 1}$.

Equation (9) indicates that for the purposes of examining the effect of parasitic resistances on the log conformance of the bipolar transistor we may ignore the collector resistance r_c, and we may lump the base resistance r_b and emitter resistance r_{ex} into a single equivalent emitter resistance term r_{ex}'. (Strictly speaking, the collector resistance can have an influence due to a phenomenon referred to as "quasi-saturation", a discussion of which is beyond the scope of this paper. This effect may be neglected if the collector resistance is kept sufficiently low.) Thus we may revise the transistor model as shown in Figure 5b.

If we substitute equation (9) into equations (3) and (4), equation (5) becomes:

$$V_o = V_{be2} - V_{be1} = V_T \ln\left(\frac{I_{out} I_{S1}}{I_{in} I_{S2}}\right) + \frac{I_{out} r'_{ex2}}{\alpha_{F2}} - \frac{I_{in} r'_{ex1}}{\alpha_{F1}}, \tag{10}$$

where r'_{ex1} and r'_{ex2} are the equivalent emitter resistances of Q1 and Q2 in Figure 1 respectively, and α_{F1} and α_{F2} are their common-base current gains. Assuming again that Q1 and Q2 are matched, isothermal devices, so that $I_{S1} = I_{S2}$, $r'_{ex1} = r'_{ex2} = r'_{ex}$, and $\alpha_{F1} = \alpha_{F2} = \alpha_F$, and solving for the input-output gain yields:

$$\frac{I_{out}}{I_{in}} = \exp\left(\frac{V_o - (I_{out} - I_{in})\frac{r'_{ex}}{\alpha_F}}{V_T}\right). \tag{11}$$

Equation (11) indicates that the gain is signal dependent in a basic Blackmer cell (Figure 3) fabricated with non-ideal devices (Figures 5a and 5b). At unity gain (when I_{out} and I_{in} are equal) the error term will be canceled. For all other gain settings the variation in gain with signal level will cause distortion of the output signal.

The VCA topology shown in Figure 4 adds four additional transistors (Q5 through Q8) and resistors (R_{C1} through R_{C4}). These devices provide a means by which to make the gain largely independent of signal level. Figure 6 shows the bottom four core transistors from the VCA

topology of Figure 4 with the addition of equivalent emitter resistances r'_{ex1}, r'_{ex2}, r'_{ex5}, and r'_{ex6} for transistors Q1, Q2, Q5, and Q6 respectively. If we assume that like devices match each other such that

$I_{S1} = I_{S2} = I_{SN}$, $I_{S5} = I_{S6} = I_{SP}$, $\alpha_{F1} = \alpha_{F2} = \alpha_{FN}$, and $\alpha_{F5} = \alpha_{F6} = \alpha_{FP}$, we may use KVL to write:

$$V_c = V_T \ln\left(\frac{I_{out}}{I_{SN}}\right) + \frac{I_{out}}{\alpha_{FN}}(r'_{ex2} + r'_{ex6}) + V_T \ln\left(\frac{I_{out}\alpha_{FP}}{I_{SP}\alpha_{FN}}\right) + I_{in}\frac{\alpha_{FP}}{\alpha_{FN}}R_{C1}$$
$$-I_{out}\frac{\alpha_{FP}}{\alpha_{FN}}R_{C2} - V_T \ln\left(\frac{I_{in}\alpha_{FP}}{I_{SP}\alpha_{FN}}\right) - \frac{I_{in}}{\alpha_{FN}}(r'_{ex1} + r'_{ex5}) - V_T \ln\left(\frac{I_{in}}{I_{SN}}\right). \quad (12)$$

Collecting terms yields:

$$V_c = 2V_T \ln\left(\frac{I_{out}}{I_{in}}\right) + \frac{I_{out}}{\alpha_{FN}}(r'_{ex2} + r'_{ex6} - \alpha_{FP}R_{C2}) - \frac{I_{in}}{\alpha_{FN}}(r'_{ex1} + r'_{ex5} - \alpha_{FP}R_{C1}). \quad (13)$$

Choosing R_{C1} and R_{C2} such that $R_{C1} = \frac{r'_{ex1} + r'_{ex5}}{\alpha_{FP}}$ and $R_{C2} = \frac{r'_{ex2} + r'_{ex6}}{\alpha_{FP}}$ causes the second and third terms of equation (13) to go to zero, leaving:

$$V_c = 2V_T \ln\left(\frac{I_{out}}{I_{in}}\right). \quad (14)$$

Solving for the current gain, $\frac{I_{out}}{I_{in}}$ yields:

$$\frac{I_{out}}{I_{in}} = \exp\left(\frac{V_c}{2V_T}\right). \quad (15)$$

Note that this expression is similar to equation (7), the ideal gain equation for the simple log-antilog circuit, except that the control voltage scaling has been halved. The signal-dependent gain effects of the parasitic base and emitter resistances of Q1, Q2, Q5, and Q6 have been canceled. This analysis may analogously extended to the top four core transistors of the VCA circuit in Figure 4, with the result that, if resistors R_{C3} and R_{C4} are chosen such that $R_{C3} = \frac{r'_{ex3} + r'_{ex7}}{\alpha_{FN}}$ and $R_{C4} = \frac{r'_{ex4} + r'_{ex8}}{\alpha_{FN}}$, then the effects of the parasitic base and emitter resistances of Q3, Q4, Q7, an Q8 are also canceled. With these "correction" resistors so chosen, the circuit of Figure 4 now behaves like the circuit in Figure 7, where all of the core transistors are assumed to have no parasitic resistance terms.

In practice, the cancellation afforded by correction resistors R_{C1}, R_{C2}, R_{C3}, and R_{C4} is not exact. While the bulk emitter resistance r_{ex} from Figure 5a is quite constant with operating current, the base resistance r_b varies with operating current due to an effect called current crowding [9]. Since the effect of the base resistance on the transistor's log conformance is a function of β_F, as shown in equation (9), variations in β_F with collector current causes further variations of the effective emitter resistance with operating current. Thus, it is desirable to minimize the parasitic resistance terms in the core transistors, particularly the base resistance, rather than rely exclusively on the cancellation effects of the correction resistors. In the current design this is accomplished by using very large geometry devices with multiple base and emitter stripes [9]. As a result, the required correction resistors are each less than 1 ohm.

2.2 Transistor Mismatches

Up to this point all of the analysis of the behavior of the VCA circuit has assumed that like devices are identically matched to one another and isothermal. The transfer function of the VCA circuit in Figure 7 is derived in Appendix A without any assumptions regarding the matching of the core transistors, and is reproduced here:

$$I_{out} = G\left[\frac{I_{in}}{2}\left(\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}} + \sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}}\right) + \sqrt{\frac{I_{in}^2}{4} + \frac{I_B^2}{G}}\left(\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}} - \sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}}\right)\right], \quad (16)$$

where I_{S1}, I_{S2}, I_{S3},...I_{S8} are the saturation currents of Q1, Q2, Q3,...Q8, respectively, $G = \exp\left(\frac{V_c}{2V_T}\right)$, and $I_B = (I_{S1}I_{S3}I_{S5}I_{S7})^{\frac{1}{4}}\exp\left(\frac{V_{BIAS}}{4V_T}\right)$. As shown in the appendix, G is the nominal VCA current gain and I_B is the dc bias current through Q2, Q3, Q5, and Q7 when the VCA is set to unity gain with no input signal.

The first term inside of the brackets represents a linear gain term (I_{in} multiplied by a constant). Note that, since all of the core transistors are nominally matched, the quantity $\left(\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}} + \sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}}\right)$ is very close to 2, confirming that G is the nominal current gain. Device mismatches merely add a slight deviation from the nominal gain to this term. The second term inside of the brackets represents even-order harmonic distortion (due to I_{in}^2) and gain-dependent dc offset (due to I_{in}^2 and I_B^2). The quantity $\left(\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}} - \sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}}\right)$ is representative of the net difference in V_{BE} matching between the top two pairs of core transistors and the bottom two pairs. This difference results in a slight current gain difference between the top log-antilog signal path and the bottom log-antilog signal path, and thus correcting this imbalance is often referred to as "symmetry adjustment". It should be noted here that, due to the "square-root of the sum-of squares" nature of the second term inside the brackets, the larger of the two terms I_{in} or I_B will very quickly tend to dominate the other. Thus, for large bias currents, (such as class A operation, where I_B is always greater than or equal to I_{in}) core transistor mismatches will primarily cause dc offset changes with gain, while for smaller bias currents these mismatches will primarily cause second harmonic distortion. The choice of bias current level also has a large effect on the circuit noise, as will be demonstrated in section 3.

Mismatches among the core transistors in an integrated VCA can arise from several sources. Systematic area mismatches in the mask are easily avoided with modern layout tools by stepping and repeating identical devices. Thermal gradients across the die can cause the transistors to operate at different temperatures. These are avoided by locating the core transistors on a line of thermal symmetry through the die, and utilizing a common-centroid layout [10]. Additionally, in the current design, components with the highest dissipation (particularly signal-dependent dissipation) are located as far as possible from the core transistors and are laid out symmetrically about the line of thermal symmetry. The remaining inevitable, random mismatches result from emitter area mismatches due to the limited resolution of the photolithography process, and from variations in the sheet resistance and junction depth of the implanted and diffused regions across the die [10]. These are minimized by making the devices as large as possible (already shown to be

beneficial for minimizing parasitic resistances) and the above-mentioned common-centroid geometry which minimizes sensitivity to process gradients across the die in the same way it minimizes the effects of thermal gradients.

The remaining random mismatches among the four pairs of core transistors must be dealt with via some sort of trimming scheme if the highest performance is to be obtained. Traditionally, this has taken the form of adding a small compensating offset voltage to the control voltage applied to either the top or bottom set of core transistors. Such an offset voltage, labeled V_{SYM}, is shown in Figure 8 connected between Q2 and Q3 in the VCA core. The effect of V_{SYM} may added to the transfer function derived in Appendix A by adding V_{SYM} to the left side of appendix equations (A2) and (A4) and carrying through a similar analysis. The resulting modified transfer function is:

$$I_{out} = G\left[\frac{I_{in}}{2}\left(\exp\left(\frac{V_{SYM}}{2V_T}\right)\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}} + \sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}}\right) + \sqrt{\frac{I_{in}^2}{4} + \frac{I_B^2}{G}}\left(\exp\left(\frac{V_{SYM}}{2V_T}\right)\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}} - \sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}}\right)\right]. \tag{17}$$

Adjusting V_{SYM} such that:

$$V_{SYM} = 2V_T \ln\left(\sqrt{\frac{I_{S1}I_{S4}}{I_{S2}I_{S3}}\frac{I_{S5}I_{S8}}{I_{S6}I_{S7}}}\right) \tag{18}$$

will cancel the second term inside the brackets in equation (17), and with it the 2nd-harmonic distortion and dc offset change with gain. Since this voltage is adjusting for V_{BE} mismatches among closely matched devices, it is no more than a few millivolts. Historically the addition of V_{SYM} has been implemented as shown in Figure 9. Typically R1 is on the order of 100 ohms or less and R2 is several hundred kohms in order to divide the power supply voltage range down to the required few millivolts. Note that it is beneficial to make this voltage divider ratio as large as possible so that changes in control voltage at the base of Q3 have minimal effect on the new adjustment voltage V_{SYM}.

Note that, due to the presence of V_T in equation (18), V_{SYM} should vary in a manner proportionate to absolute temperature (PTAT) in order for the transistor mismatch correction to hold for all operating temperatures. The current design incorporates an on-chip symmetry trim technique (patent pending) which provides correct adjustment over changes in device temperature. As shown in Figure 10, a bidirectional current source proportional to $\frac{V_T}{R}$, where R is a trimmable, on-chip resistor, is used to generate a current through R1. At wafer test the direction and magnitude of the current source are adjusted to correct for core transistor mismatches. R1 is nominally 27 ohms in the current design. As this resistance appears directly in series with the r_b of Q2, it is important that it be low in value. Additionally, correction resistor R_{C2} in Figure 4 is adjusted to minimize log errors introduced by R1.

Wafer-level trimming is subject to shifts during the die packaging process. Production devices are graded after packaging according to how well the trim survives packaging. Prime grade devices exhibit THD less than .01% at unity gain for a 1 V rms input. This can be shown to correspond to a net V_{BE} mismatch between the top four core transistors and the bottom four core transistors of +/-35 uV at room temperature. The lowest cost devices exhibit THD less than

.05% under the same conditions, corresponding to a net V_{BE} mismatch of +/-175uV. And, for those applications which demand it, an external fine trim may be added as shown in Figure 9.

2.3 Input Amplifier Non-Linearity

The VCA input amplifier, shown as OA1 in Figure 10 and preceding figures, must drive the nonlinear feedback loop presented by the core transistors and must remain stable under the varying feedback conditions created as the VCA gain is altered. (This is in contrast to the output current-to-voltage conversion amplifier OA2, which is always at unity closed loop gain). At high frequencies, where overall loop gain is rolling off due to stability considerations, nonlinearity in OA1 can begin to dominate the overall distortion performance of the VCA.

One aspect of the input amplifier that can influence its distortion behavior when driving the VCA core is its output impedance. Figure 11 shows the two extreme cases. In Figure 11a, OA1 is shown as an ideal voltage gain stage with zero output impedance and gain A. The loop transmission around OA1 will be:

$$LT_{11a} = \frac{-AR_{in}}{r_{eq}(G+1)} \tag{19}$$

where:

$$r_{eq} = \frac{1}{\frac{I_{c1}}{2V_T} + \frac{I_{c2}}{2V_T} + \frac{I_{c3}}{2V_T} + \frac{I_{c4}}{2V_T}} \text{ and } G = \exp\left(\frac{V_c}{2V_T}\right) \text{ (the VCA gain).}$$

Since the collector currents of the core transistors are signal-dependent, particularly in a class AB design, the loop transmission will be signal dependent. This signal-dependent variation in open loop gain will cause distortion that will be reduced by negative feedback. However, at high frequencies, and at high VCA gains (large G), when overall loop gain is reduced, this distortion can dominate the overall performance.

In contrast, Figure 11b shows OA1 as an ideal transconductance amplifier with a high impedance current output and transconductance G_m. The loop transmission of this version of the VCA circuit will be:

$$LT_{11b} = \frac{-G_m R_{in}}{G+1} \tag{20}$$

In this case the loop transmission is signal independent, eliminating the distortion mechanism shown previously.

Figure 12 shows a simplified schematic of the transconductance amplifier used in the current design along with the simplified VCA core. Transistors Q9-Q12 and their associated circuitry make up a differential voltage gain stage, with C1 providing dominant pole compensation. The output of this stage is buffered by emitter follower Q13, and converted to an output current to drive the VCA core by the Q14/R5 combination. Q14 is heavily biased into class A, typically with 2 mA of collector current, so that the transconductance of this stage is dominated by R5. Capacitor C2 adds a 10 MHz zero to the loop transmission which adds phase lead to mitigate against the lag added by the base-emitter capacitances of the core transistors working against their dynamic emitter resistances. Resistor R6 adds a 2 MHz zero to the loop transmission to cancel

the pole created by R_{in} (typically 20 kohms) and the capacitance seen at the junction of the collectors of Q1 and Q3. This capacitance is dominated by the collector-base junction capacitance of these large geometry devices. In a typical junction-isolated (JI) IC process there would be an additional capacitance at this node due to the collector-substrate isolation junction. This capacitance can be five to ten times as large as the collector-base junction capacitance of the device [9]. The current design utilizes a dielectrically-isolated (DI) process, eliminating the collector-substrate junction capacitance.

The resulting input amplifier exhibits a gain-bandwidth product of 20 MHz with the typical Rin value of 20 kohms. This, along with the linear behavior of the transconductance amplifier result in negligible increase in VCA distortion at high audio frequencies for VCA gains up to 20 dB.

Slew rate capability is determined by the maximum rate of change of current at the collector of Q14. The VCA gain setting determines how this current is split between the input and output sides of the core. This results in a maximum voltage slew rate of the input and output voltages that can be approximated by the following equations:

$$SR_{IN} = \frac{I_2 R_{in}}{2C1R5(1+G} \tag{21}$$

and

$$SR_{OUT} = \frac{I_2 R_{out} G}{2C1R5(1+G)}. \tag{22}$$

At unity gain, with $R_{in} = R_{out} = 20k\Omega$, the maximum input and output slew rates are each 12.5 V/us (assuming that output amplifier OA2 does not otherwise limit the output slew rate).

3 VCA NOISE PERFORMANCE

Assuming the surrounding circuitry is well-designed, at moderate gain or attenuation settings the noise performance with no input signal of a log-antilog VCA is determined by the collector current shot noise of the core transistors. The level of this noise is controlled by the bias current in the core transistors. As will be shown in more detail, higher bias currents cause higher noise. However, all things being equal, higher bias currents also tend to reduce distortion, particularly at high frequencies (the situation is analogous to crossover distortion in amplifiers). Thus, there is a tradeoff between the reduction in distortion gained by raising the bias current to the level of the maximum expected signal current (class A operation) and the increase in noise that this causes. Section 3.1 examines the noise behavior with no input signal in detail.

When signal currents are added to the bias currents in the core transistors, the noise level changes. The changes in current levels in the core transistors are clearly much greater when the bias current is a relatively small fraction of the maximum input signal. However, it will be demonstrated in section 3.2 that, with proper care in the design of the core transistors, and in the circuitry driving the VCA control port, these effects can be minimized.

3.1 Noise with No Input Signal

Referring to Appendix B, the noise analysis of the VCA circuit, we can write the equation for the total noise at the output of the VCA when $I_{in} = 0$. Substituting equations (B2), (B17), (B27), (B33), and (B34) into equation (B35) under this condition yields:

$$e_{ntotal} = \sqrt{R_{out}^2\left[\left(\frac{G}{R_{in}}e_{ninput}\right)^2 + 2qI_B\left(G^{\frac{1}{2}} + G^{\frac{3}{2}}\right) + \left(\frac{I_B}{V_T}\right)^2 G4kT(r_{bn} + r_{bp})\right] + e_{noutput}^2} \quad . \tag{23}$$

The first term inside of the brackets is due to the equivalent input noise sources of the input amplifier and the input voltage-to-current conversion resistor R_{in}. In the current design e_{ninput} is on the order of 28 nV/$\sqrt{Hz}$ assuming that $R_{in} = 20$ kΩ. The second term inside of the brackets is due to shot noise in the core transistors. The third term inside of the brackets is due to thermal noise originating in the base resistances of the core transistors. These resistances are on the order of ten ohms in the current design. The last term (outside of brackets) is noise due to the output current-to-voltage conversion amplifier. This amplifier is external to the IC in the present design, but its noise performance is usually dominated by R_{out} (again typically 20 kΩ) and thus is on the order of 20 nV/$\sqrt{Hz}$. Note that under no-signal conditions, noise at the VCA control terminals does not contribute to the output noise.

The bias current I_B for the current design was set to 20 uA based on simulations which suggested that this level of bias current was adequate to prevent any rise in distortion at high frequencies for gains up to +20 dB. (The V_{BIAS} generator circuit used to set I_B is described in reference [11]). With this value for I_B, $R_{in} = R_{out} = 20$ kΩ, and $r_{bp} = r_{bn} = 10$ Ω, equation (23) becomes:

$$e_{ntotal} =$$

$$\sqrt{G^2\left(28\text{nV}/\sqrt{\text{Hz}}\right)^2 + \left(G^{\frac{1}{2}} + G^{\frac{3}{2}}\right)\left(50.6\text{ nV}/\sqrt{\text{Hz}}\right)^2 + G\left(8.7\text{ nV}/\sqrt{\text{Hz}}\right)^2 + \left(20\text{nV}/\sqrt{\text{Hz}}\right)^2} \quad . \tag{24}$$

At unity gain this evaluates to 80 nV/$\sqrt{Hz}$, or -98.9 dBV in a 20 kHz bandwidth. The second term on the right-hand side of equation (24), the collector current shot noise contribution, dominates the expression for VCA gains between approximately -30 dB and +20 dB. It varies approximately with $G^{\frac{3}{4}}$ for gains greater than unity, and with $G^{\frac{1}{4}}$ for gains less than unity. At gains higher than +20 dB, the first term, the input amplifier noise contribution, begins to dominate the expression. It varies directly with the VCA gain, as will any noise present at the input due to previous circuitry. At gains lower than -30 dB, the last term, due to the output amplifier noise, begins to dominate and ultimately sets the noise floor achievable with the VCA at maximum attenuation.

It is interesting to contrast this noise behavior with that of the same circuit with I_B set for class A operation. Setting I_B to 750 uA allows peak input voltages of +/-15 V under class A conditions with $R_{in} = R_{out} = 20$ kΩ. Substituting this condition into equation (23) yields:

$e_{ntotal} =$

$$\sqrt{G^2\left(28nV/\sqrt{Hz}\right)^2+\left(G^{\frac{1}{2}}+G^{\frac{3}{2}}\right)\left(310\ nV/\sqrt{Hz}\right)^2+G\left(326\ nV/\sqrt{Hz}\right)^2+\left(20nV/\sqrt{Hz}\right)^2}\ . \tag{25}$$

At unity gain this evaluates to 547 $nV/\sqrt{Hz}$, or -82.2 dBV in a 20 kHz bandwidth. Note that the contribution due to the core transistor base resistances, which was negligible in the class AB case, is now a very important factor in the noise performance. This term varies directly with I_B, whereas the shot noise contribution varies with $\sqrt{I_B}$.

3.2 Variation of Noise with Signal

As shown in Appendix B, several components of the total output noise of the VCA are dependent on the level of the input signal. We shall examine each of these components in turn.

Appendix B equation (B16) shows the output noise current density due to shot noise in the core transistors, and is reproduced below:

$$i_{nouts} = \sqrt{2q(G+G^2)\sqrt{\frac{I_{in}^2}{4}+\frac{I_B^2}{G}}}\ . \tag{26}$$

This equation indicates that the output noise contribution due to shot noise in the core transistors varies with $\sqrt{I_{in}}$, the instantaneous input current, for a given bias current and gain.

Appendix B equation (B26) shows the output noise current density due to the core transistor base resistances, and is reproduced below:

$$i_{noutr_b} = \frac{G}{V_T}\sqrt{\left(I_{in}^2+\frac{2I_b^2}{G}\right)4kT\left(\frac{r_{bp}+r_{bn}}{2}\right)}\ . \tag{27}$$

This equation indicates that the output noise contribution due to the base resistors varies directly with I_{in}, the instantaneous input current, for a given bias current and gain.

Appendix B equation (B32) shows the output noise current density due to external noise sources at the VCA gain-control terminals and is reproduced below:

$$i_{noutvc} = \frac{I_{in}G}{2V_T}\sqrt{e_{nv_{vp}}^2+e_{nv_{en}}^2}\ . \tag{28}$$

This equation indicates that voltage noise sources at the VCA gain-control terminals contribute to the output noise only when there is an input signal present, and that this contribution is proportional to the instantaneous input level.

Output noise due to the first two sources listed above is unavoidable. Instantaneous modulation of these noise contributions by the input signal can be made much less apparent by increasing the bias current to levels that are comparable to the maximum signal level. This is done at the expense of having much higher noise levels all of the time, as shown in the previous section.

Instantaneous modulation of the output noise by the input signal due to the third source, noise on the control port, is avoidable. However, in the author's experience, this aspect of designing application circuits which utilize VCAs is far too often overlooked. A voltage noise density of more than a few $nV/\sqrt{Hz}$ at either of the control terminals can easily dominate the noise behavior at high signal levels. This is due to the fact that the shot noise contribution, though dominant under no-signal conditions, grows only with $\sqrt{I_{in}}$ and the contribution due to the base resistances, though it is proportional to I_{in}, is made quite small to begin with due to the large transistor geometries. A comparison of the noise modulation behavior of the current design with differing amounts of noise at the control terminals is shown in section 5.

4 CONTROL VOLTAGE FEEDTHROUGH

As shown in equation (17), mismatches in the core transistors can lead to an output offset current proportional to $I_B\sqrt{G}$. Adding a compensating voltage as indicated in equation (18) simultaneously minimizes this offset current and the distortion mechanism caused by transistor mismatches.

The other major cause of output offset variation with changes in gain is any current present at the input. DC offsets present at the output of previous stages, and the input offset voltage of the VCA input amplifier will create input currents which will reflect to the output multiplied by the VCA gain G. Fortunately, these sources of offset change with gain are eliminated by merely ac-coupling the input to the VCA.

The input bias current of the VCA input amplifier is also an input current that gets reflected to the output via the VCA gain G. To minimize this the input amplifier topology in Figure 12 is modified with the addition of an input bias-current cancellation circuit. This circuit is described in detail in reference [12]. This results in typical input bias currents of a few nanoamperes, without the use of FETs.

High frequency signals at the control port (such as those in fast-opening noise gates) can couple directly to the input and output nodes via the collector-base capacitances of the primary core transistors. Driving the VCA control port differentially provides some reduction in this feedthrough, but, since the collector base capacitances of the NPN and PNP transistors are not matched, this is only partially effective. One technique that has been used successfully is to couple an inverted replica of the control voltage signal directly to the summing junction of the output amplifier via a small capacitor. Once the capacitor value is empirically chosen, it need not be altered as the collector-base capacitances are quite constant from device to device.

5 PERFORMANCE DATA

As mentioned above, the current design is implemented in a 25 V DI process that includes NPN transistors with f_t of 600 MHz and vertical PNP transistors with f_t of 500 MHz.

The following performance data on production samples of the current design was taken with the application circuit shown in Figure 14 using an Audio Precision System One and DCX-127. Figures 15, 16, and 17 show THD+N versus input level at 0 dB, +15 dB, and -15 dB respectively. Each figure contains curves for each of the three selection grades based on wafer-stage symmetry

trim accuracy (the top three curves), as well as a curve for performance with an external symmetry trim (bottom curve). An analyzer bandwidth of 22 kHz was used for these measurements.

Figure 18 shows THD+N versus frequency for a 1 Vrms input level at unity gain. The top curve is taken with an 80 kHz analyzer bandwidth in order to include high frequency harmonics. The bottom curve was taken with a 20 kHz analyzer bandwidth, demonstrating that the 80 kHz bandwidth measurement is dominated by noise. Figures 19 and 20 are similar curves taken at +15 dB gain with a -10 dBV input level and -15 dB gain with a +10 dBV input level, respectively. These curves were taken with an 80 kHz bandwidth, and the VCA symmetry was externally trimmed.

Figure 21 shows a curve of typical offset change with gain for the three selection grades (top three curves), as well as a curve for performance with an external symmetry trim (bottom curve).

Figure 22 is a plot of 22 kHz-bandwidth noise versus VCA gain (with no input signal).

Figure 23 is a plot of the 22 kHz-bandwidth noise floor versus input signal level at unity gain. This test was performed using a 20 Hz input signal and plotting the output of the THD+N analyzer using its 400 Hz highpass and 22 kHz lowpass filters. Thus, any distortion products due to the 20 Hz input signal are removed by the highpass filter, leaving the analyzer to read the noise floor alone. Note that, at the highest input levels, the noise floor remains more than 100 dB below the signal level.

By contrast, Figure 24 shows the same plot, except that U4, the low-noise AD797 control voltage buffer opamp has been replaced with a TL081 FET-input opamp with significantly higher voltage noise. The effects of careless design of the control voltage circuitry are obvious. As the signal at the VCA control port multiplies the incoming audio signal, designers should treat this signal as carefully as they do the audio signal path.

In the areas of distortion at gains other than unity, and distortion at high frequencies at all gains, the present design is notably superior to a previous design widely used throughout the professional audio industry [13]. Additionally, the addition of wafer-stage trimming of symmetry eliminates the need for an external trimpot and the adjustment time during production test for many applications.

6 CONCLUSIONS

The design of a monolithic VCA IC with exponential gain control has been described. A complementary log-antilog topology that allows for correction for parasitic core-transistor resistances was chosen for its simple signal path and small die-area requirement.

The major sources of distortion for such devices are transistor mismatches, parasitic transistor base and emitter resistances, and input-amplifier non-linearity. Transistor mismatches are minimized through careful layout and a wafer-level trim technique which eliminates the need for an external trimpot in many applications. Large geometry core transistors, along with the correction afforded by the core topology, were used to minimize errors due to transistor base and emitter resistances. A transconductance amplifier as the input amplifier for the VCA minimizes nonlinearity at high frequencies where open loop gain is rolling off due to stability considerations.

The use of a dielectrically-isolated IC process allows increased gain-bandwidth product over a junction-isolated IC process, also decreasing distortion at high frequencies.

Noise at the output of the VCA with no input signal present was shown to be dominated by shot noise due to collector current in the core transistors for the most heavily-used gain range of -30 dB to +20 dB. For gains greater than +20 dB, the output noise was shown to become dominated by noise sources at the VCA input. For gains less than -30 dB, the output noise was shown to become dominated by noise sources in the output amplifier circuit. It was shown that increasing the bias current in the core transistors to the levels required for class A operation would increase the noise floor by 16 dB at unity gain.

The output noise of the VCA was shown to be dependent on the input signal level. Three sources of signal-dependent noise were identified: shot noise due to the core transistors, thermal noise due to the base resistances of the core transistors, and voltage noise at the control terminals of the VCA. The last of these three sources was shown to have a great influence on the noise performance of the VCA at high signal levels. It was demonstrated in the performance measurements that, with proper design of the control voltage driving circuitry, modulation of the VCA noise floor by the input signal could be minimized.

Control voltage feedthrough at low frequencies was shown to be caused primarily by transistor mismatches in the VCA core and input bias currents of the VCA input amplifier. It was demonstrated that trimming of transistor mismatches simultaneously nulls both distortion and control-voltage feedthrough. An input bias-current cancellation circuit was shown to be effective in minimizing gain-dependent offsets due to bias currents.

Control voltage feedthrough at high frequencies was shown to be caused by coupling of the control signal to the VCA output via core transistor collector-base capacitances. Techniques to minimize this effect were suggested.

Performance data on the completed design were presented showing the efficacy of the techniques described.

7 ACKNOWLEDGMENT

The author would like to acknowledge the contributions of David Blackmer and David Welland, upon whose prior work this design was based. He would also like to thank Les Tyler for his assistance in the preparation of this paper.

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Appendix A

DERIVATION OF VCA TRANSFER FUNCTION

By inspection of Figure 7, using KVL:

$$V_c = V_{BIAS} - 2V_T \ln\left(\frac{I_{c3}}{\sqrt{I_{S3}I_{S7}}}\right) - 2V_T \ln\left(\frac{I_{c1}}{\sqrt{I_{S1}I_{S5}}}\right), \tag{A1}$$

$$V_c = -V_{BIAS} + 2V_T \ln\left(\frac{I_{c4}}{\sqrt{I_{S4}I_{S8}}}\right) + 2V_T \ln\left(\frac{I_{c2}}{\sqrt{I_{S2}I_{S6}}}\right), \tag{A2}$$

$$V_c = 2V_T \ln\left(\frac{I_{c4}}{\sqrt{I_{S4}I_{S8}}}\right) - 2V_T \ln\left(\frac{I_{c3}}{\sqrt{I_{S3}I_{S7}}}\right), \tag{A3}$$

$$V_c = 2V_T \ln\left(\frac{I_{c2}}{\sqrt{I_{S2}I_{S6}}}\right) - 2V_T \ln\left(\frac{I_{c1}}{\sqrt{I_{S1}I_{S5}}}\right), \tag{A4}$$

where: $V_T = \frac{kT}{q}$ and I_{S1}, I_{S2}, I_{S3},...I_{S8} are the saturation currents of Q1, Q2, Q3,...Q8, respectively, including emitter area effects.

From KCL:

$$I_{c3} + I_{in} = I_{c1}, \tag{A5}$$

$$I_{c4} + I_{out} = I_{c2}. \tag{A6}$$

Rearranging equation (A1):

$$V_c - V_{BIAS} = -2V_T \ln\left(\frac{I_{c3}I_{c1}}{\sqrt{I_{S3}I_{S7}I_{S1}I_{S5}}}\right). \tag{A7}$$

Substituting for I_{c1} in equation (A7) using equation (A5):

$$V_c - V_{BIAS} = -2V_T \ln\left(\frac{I_{c3}^2 + I_{c3}I_{in}}{\sqrt{I_{S3}I_{S7}I_{S1}I_{S5}}}\right), \tag{A8}$$

and rearranging terms leads to:

$$I_{c3}^2 + I_{c3}I_{in} = \sqrt{I_{S3}I_{S7}I_{S1}I_{S5}}\ \exp\left(\frac{V_{BIAS} - V_c}{2V_T}\right) \tag{A9}$$

Here, for neatness and convenience, we will define two variables. The first is the familiar expression for the current gain of the VCA. The significance of the second will become clear later. Let:

$$G = \exp\left(\frac{V_c}{2V_T}\right), \tag{A10}$$

and

$$I_B = (I_{S1}I_{S3}I_{S5}I_{S7})^{\frac{1}{4}}\exp\left(\frac{V_{BIAS}}{4V_T}\right). \tag{A11}$$

Substituting these variables into equation (A9),

$$I_{c3}^2 + I_{c3}I_{in} = \frac{I_B^2}{G}, \tag{A12}$$

and solving for I_{c3} yields:

$$I_{c3} = -\frac{I_{in}}{2} \pm \sqrt{\frac{I_{in}^2}{4} + \frac{I_B^2}{G}}. \tag{A13}$$

For proper circuit operation, I_1 must be positive, and we know that the quantity under the radical symbol is positive since G is always positive. Thus, given that I_B is nonzero, we may choose one root:

$$I_{c3} = -\frac{I_{in}}{2} + \sqrt{\frac{I_{in}^2}{4} + \frac{I_B^2}{G}}. \tag{A14}$$

Substituting equation (A14) into equation (A5) yields:

$$I_{c1} = \frac{I_{in}}{2} + \sqrt{\frac{I_{in}^2}{4} + \frac{I_B^2}{G}}. \tag{A15}$$

It may be noted here that, when I_{in}=0 and G=1, I_{c3} and I_{c1} are equal to I_B. Thus, I_B is the unity-gain standby bias current in the input side of the gain cell.

Solving equation (A3) for I_3 and substituting for I_{c3} using equation (A14):

$$I_{c4} = I_{c3}\sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}}\exp\left(\frac{V_c}{2V_T}\right) = GI_{c3}\sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}} = G\sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}}\left(-\frac{I_{in}}{2} + \sqrt{\frac{I_{in}^2}{4} + \frac{I_B^2}{G}}\right). \tag{A16}$$

Solving equation (A4) for I_4 and substituting for I_2 using equation (A15):

$$I_{c2} = I_{c1}\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}}\exp\left(\frac{V_c}{2V_T}\right) = GI_{c1}\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}} = G\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}}\left(\frac{I_{in}}{2} + \sqrt{\frac{I_{in}^2}{4} + \frac{I_B^2}{G}}\right) \tag{A17}$$

Substituting equations (A16) and (A17) into equation (A6) and solving for I_{out} yields:

$$I_{out} = \left[G\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}}\left(\frac{I_{in}}{2} + \sqrt{\frac{I_{in}^2}{4} + \frac{I_B^2}{G}}\right)\right] - \left[G\sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}}\left(-\frac{I_{in}}{2} + \sqrt{\frac{I_{in}^2}{4} + \frac{I_B^2}{G}}\right)\right]. \tag{A18}$$

Collecting terms:

$$I_{out} = G\left[\frac{I_{in}}{2}\left(\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}} + \sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}}\right) + \sqrt{\frac{I_{in}^2}{4} + \frac{I_B^2}{G}}\left(\sqrt{\frac{I_{S2}I_{S6}}{I_{S1}I_{S5}}} - \sqrt{\frac{I_{S4}I_{S8}}{I_{S3}I_{S7}}}\right)\right]. \tag{A19}$$

Note that the first term in the brackets is a linear gain term (I_{in} multiplied by a constant) and the second term represents second-harmonic distortion and dc offset. When the core transistor pairs are matched such that $I_{S1} = I_{S2}$, $I_{S3} = I_{S4}$, $I_{S5} = I_{S6}$, and $I_{S7} = I_{S8}$ then equation (A19) reduces to:

$$I_{out} = GI_{in}. \tag{A20}$$

Appendix B

VCA NOISE ANALYSIS

Figure 13 shows a simplified schematic of the current VCA showing all of the important noise sources. These sources are defined below:

Symbol	Definition
e_{nOA1}	Equivalent input noise voltage density of input amplifier OA1.
i_{nOA1}	Equivalent input noise current density of input amplifier OA1.
$e_{nR_{in}}$	Thermal noise voltage density due to R_{in} $\left(\sqrt{4kTR_{in}}\right)$.
i_{nsx}	Collector shot noise current density of transistor QX $\left(\sqrt{2qI_{cx}}\right)$.
$e_{nr_{bX}}$	Thermal noise voltage density due to r_b of transistor QX $\left(\sqrt{4kTr_{bX}}\right)$.
$e_{nV_{ep}}$	Noise voltage density present in positive sense control voltage source.
$e_{nV_{en}}$	Noise voltage density present in negative sense control voltage source.
e_{nOA2}	Equivalent input noise voltage density of output amplifier OA2.
i_{nOA2}	Equivalent input noise current density of output amplifier OA2.
$e_{nR_{out}}$,	Thermal noise voltage density due to R_{out} $\left(\sqrt{4kTR_{out}}\right)$.

The noise sources due to the input amplifier OA1 and input resistor R_{in} may be combined into a single equivalent noise source, e_{nin}, defined below:

$$e_{ninput} = \sqrt{e_{nOA1}^2 + e_{nR_{in}}^2 + i_{nOA1}^2 R_{in}^2}\ . \tag{B1}$$

This voltage noise source at the VCA input will reflect to an output noise voltage via the VCA voltage gain:

$$e_{nout1} = e_{ninput}\left(\frac{R_{out}}{R_{in}}\right)\exp\left(\frac{V_c}{2V_T}\right) = e_{ninput}\left(\frac{R_{out}}{R_{in}}\right)G. \tag{B2}$$

The shot noise current density of the core transistors is (ignoring base current errors):

$$i_{ns1} = i_{ns5} = \sqrt{2qI_{c1}}\ , \tag{B3}$$

$$i_{ns2} = i_{ns6} = \sqrt{2qI_{c2}}\ , \tag{B4}$$

$$i_{ns3} = i_{ns7} = \sqrt{2qI_{c3}}\ , \tag{B5}$$

$$i_{ns4} = i_{ns8} = \sqrt{2qI_{c4}} \tag{B6}$$

where I_{c1}, I_{c2}, I_{c3}, and I_{c4} are the collector currents defined in Appendix A equations A13 through A17, and q is the electron charge.

The noise current at the collectors of the four primary VCA core transistors Q1 through Q4 will be 3 dB less than that due to a single transistor operating at the same collector current due to the presence of a diode-connected transistor (Q5 through Q8) in series with the emitter of each of the primary transistors. This is due to the fact that while the diode connected transistors add an equal, uncorrelated noise source to that of the primary transistors, they also add 6 dB of emitter degeneration to the primary transistors. For example, the shot noise current density at the collector of Q1 due to Q1 and Q5 will be:

$$i_{nsc1} = \sqrt{qI_{c1}} \; . \tag{B7}$$

Similarly, for the other three quadrants of VCA core:

$$i_{nsc2} = \sqrt{qI_{c2}} \; , \tag{B8}$$

$$i_{nsc3} = \sqrt{qI_{c3}} \; , \tag{B9}$$

$$i_{nsc4} = \sqrt{qI_{c4}} \; . \tag{B10}$$

From Appendix A equations (A16) and (A17), and assuming that all of the core transistors are matched (or that symmetry has been properly trimmed), we can state that:

$$I_{c2} = GI_{c1} \tag{B11}$$

and

$$I_{c4} = GI_{c3} \; . \tag{B12}$$

Substituting equations (B11) and (B12) in to equations (B8) and (B10) respectively yields:

$$i_{nsc2} = \sqrt{qGI_{c1}} \tag{B13}$$

and

$$i_{nsc4} = \sqrt{qGI_{c3}} \; . \tag{B14}$$

The collector currents on the input side of the VCA reflect to the output current node via the VCA gain G, while the collector currents on the output side add directly to the output current. Thus we may calculate the total output noise current density due to the core transistor shot noise as:

$$i_{nouts} = \sqrt{(Gi_{nsc1})^2 + (Gi_{nsc3})^2 + i_{nsc2}^2 + i_{nsc4}^2} = \sqrt{q(G+G^2)(I_{c1}+I_{c3})} \; . \tag{B15}$$

Substituting for I_{c1} and I_{c2} using Appendix A equations (A14) and (A15) respectively yields:

$$i_{nouts} = \sqrt{2q(G+G^2)\sqrt{\frac{i_{in}^2}{4} + \frac{i_B^2}{G}}} \; . \tag{B16}$$

This noise current density will be reflected to the output voltage via R_{out} as shown below:

$$e_{nout2} = R_{out} i_{nouts} = R_{out} \sqrt{2q(G+G^2)\sqrt{\frac{I_{in}^2}{4} + \frac{I_B^2}{G}}} \quad . \tag{B17}$$

The thermal noise due to the base resistances in the core transistors will be converted to a noise current at the collectors of the primary core transistors via the degenerated transconductance of the combined primary transistor and diode transistor, $\frac{I_{cx}}{2V_T}$. Thus, the noise current density due to the base resistances at each of the core transistors is

$$i_{nr_bc1} = \sqrt{\left(\frac{e_{nr_{b1}} I_{c1}}{2V_t}\right)^2 + \left(\frac{e_{nr_{b5}} I_{c1}}{2V_t}\right)^2} \quad , \tag{B18}$$

$$i_{nr_bc2} = \sqrt{\left(\frac{e_{nr_{b2}} I_{c2}}{2V_t}\right)^2 + \left(\frac{e_{nr_{b6}} I_{c2}}{2V_t}\right)^2} \quad , \tag{B19}$$

$$i_{nr_bc3} = \sqrt{\left(\frac{e_{nr_{b3}} I_{c3}}{2V_t}\right)^2 + \left(\frac{e_{nr_{b7}} I_{c3}}{2V_t}\right)^2} \quad , \tag{B20}$$

$$i_{nr_bc4} = \sqrt{\left(\frac{e_{nr_{b4}} I_{c4}}{2V_t}\right)^2 + \left(\frac{e_{nr_{b8}} I_{c4}}{2V_t}\right)^2} \quad , \tag{B21}$$

Substituting equations (B11) and (B12) into (B16) and B(18) respectively yields:

$$i_{nr_bc2} = \sqrt{\left(\frac{e_{nr_{b2}} G I_{c1}}{2V_t}\right)^2 + \left(\frac{e_{nr_{b6}} G I_{c1}}{2V_t}\right)^2} \tag{B22}$$

and

$$i_{nr_bc4} = \sqrt{\left(\frac{e_{nr_{b4}} G I_{c3}}{2V_t}\right)^2 + \left(\frac{e_{nr_{b8}} G I_{c3}}{2V_t}\right)^2} \quad . \tag{B23}$$

These noise current densities may also be reflected to the output current node in the same manner as for the shot noise currents. Thus:

$$i_{noutr_b} = \sqrt{(G i_{nr_bc1})^2 + (G i_{nr_bc3})^2 + i_{nr_bc2}^2 + i_{nr_bc4}^2} \quad . \tag{B24}$$

Assuming that the base resistances of the four NPN transistors match, and that the base resistances of the four PNP transistors match, such that $r_{b1} = r_{b2} = r_{b7} = r_{b8} = r_{bn}$ and $r_{b3} = r_{b4} = r_{b5} = r_{b6} = r_{bp}$, and substituting equations (B18), (B19), (B22), and (B23) into equation (B24) yields:

$$i_{noutr_b} = \frac{G}{V_T} \sqrt{\left(I_{c1}^2 + I_{c3}^2\right)\left(\frac{e_{nr_{bn}}^2 + e_{nr_{bp}}^2}{2}\right)} \tag{B25}$$

where: $e_{nr_{bn}} = \sqrt{4kTr_{bn}}$ and $e_{nr_{bp}} = \sqrt{4kTr_{bp}}$.

Substituting for I_{c1} and I_{c3} using equations (A14) and (A15) respectively yields:

Figure 1. Basic Log-Antilog Circuit.

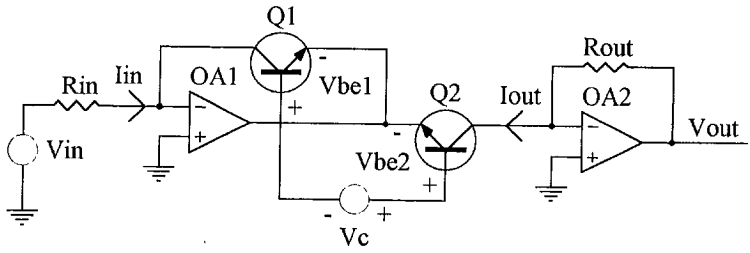

Figure 2. All NPN Log-Antilog VCA.

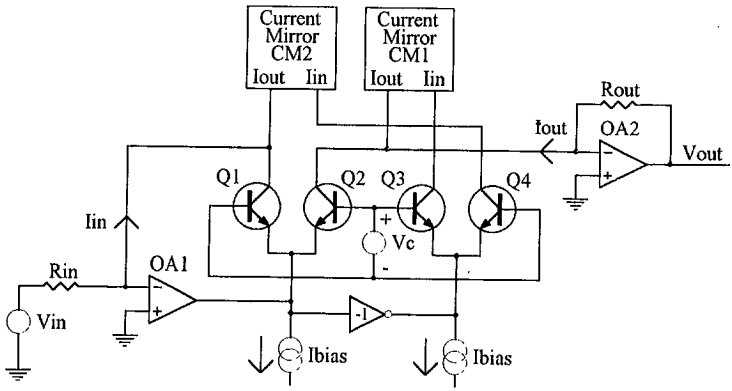

Figure 3. Basic Complementary Log-Antilog VCA.

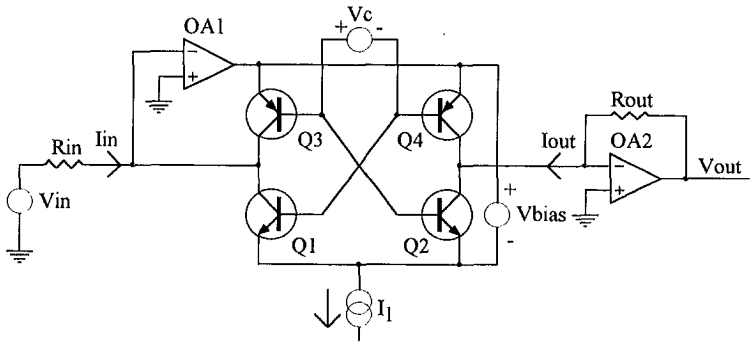

Figure 4. Complementary Log-Antilog VCA Used in Current Design.

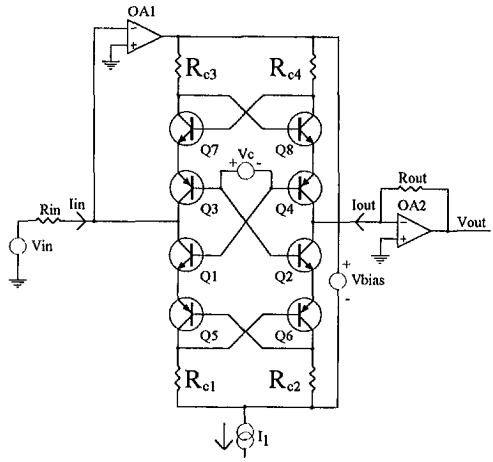

Figure 5a. Transistor with Parasitic Resistances (left)
Figure 5b. Transistor with Equivalent Emitter Resistance (right, see text).

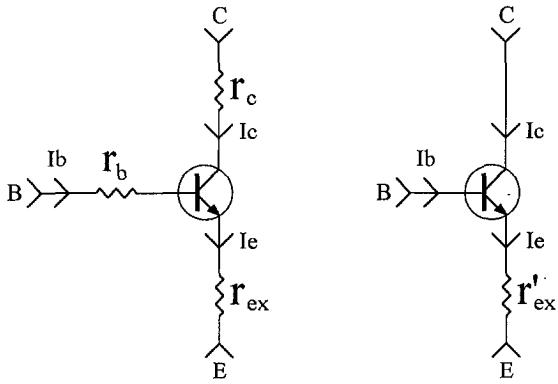

Figure 6. Bottom Half of VCA Core Showing Equivalent Emitter Resistances.

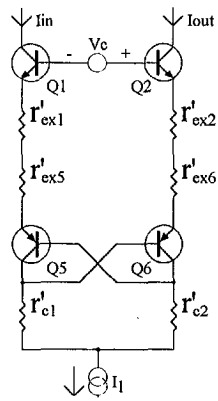

Figure 7. VCA Equivalent Circuit After Correction of Resistive Errors (see text).

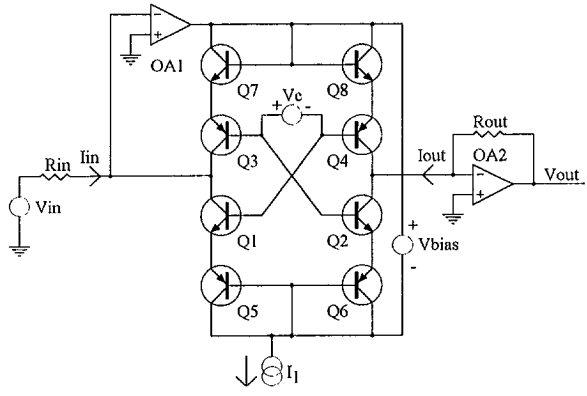

Figure 8. VCA Equivalent Circuit With Symmetry Correction Voltage.

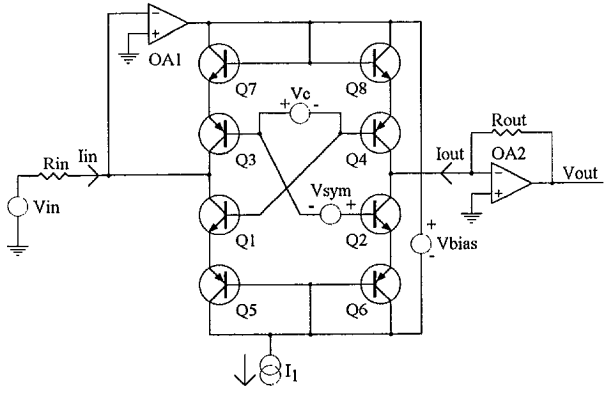

Figure 9. VCA Equivalent Circuit with External Symmetry Trim.

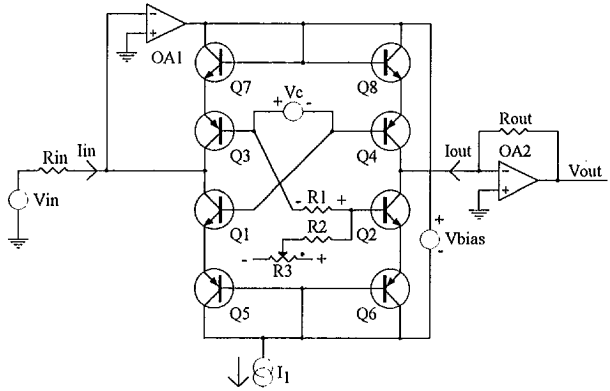

Figure 10. VCA Equivalent Circuit with Temperature-Dependent Current Source for Symmetry Adjustment.

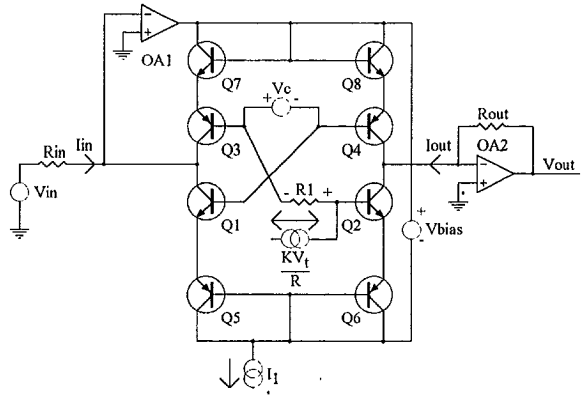

Figure 11a. VCA Equivalent Circuit with Voltage Amp Drive (see text).

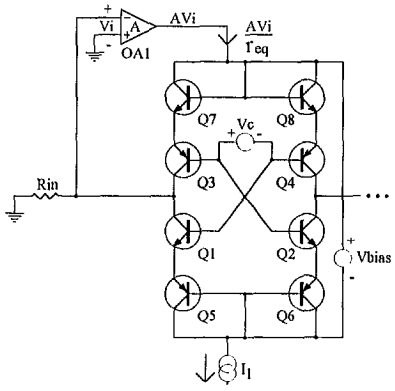

Figure 11b. VCA Equivalent Circuit with Transconductance Drive (see text).

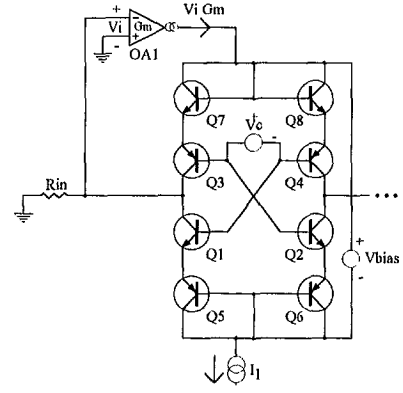

Figure 12. Simplified Equivalent Schematic of VCA IC Input Amplifier.

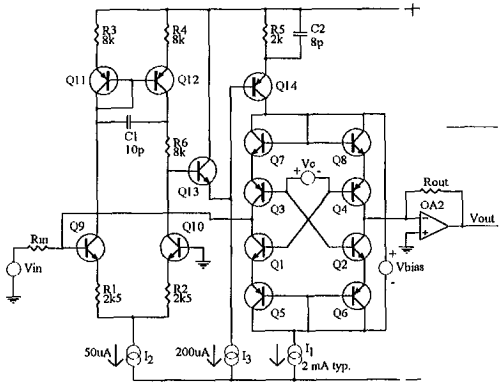

Figure 13. VCA Circuit with Equivalent Noise Sources.

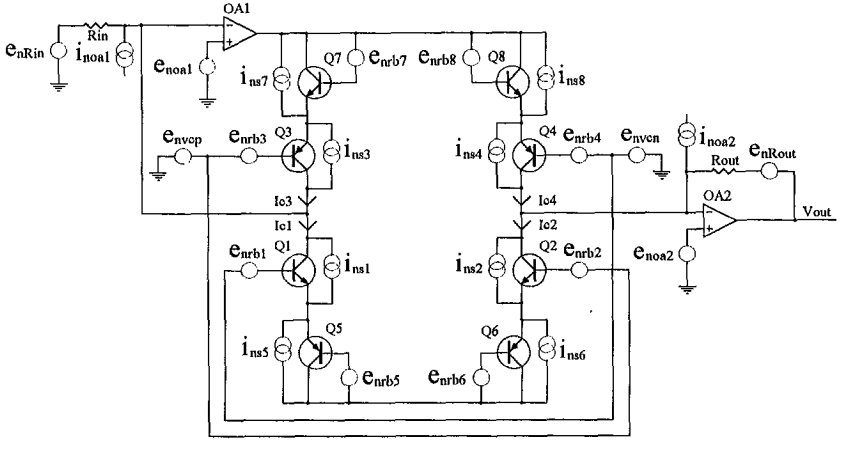

Figure 14. Application Circuit Used for Performance Measurements.

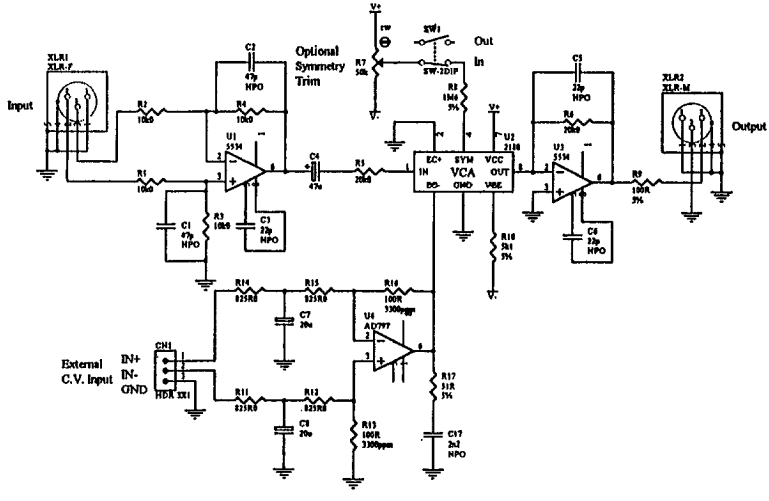

Figure 15. THD+N vs. Input Level at 0 dB Gain (see text).

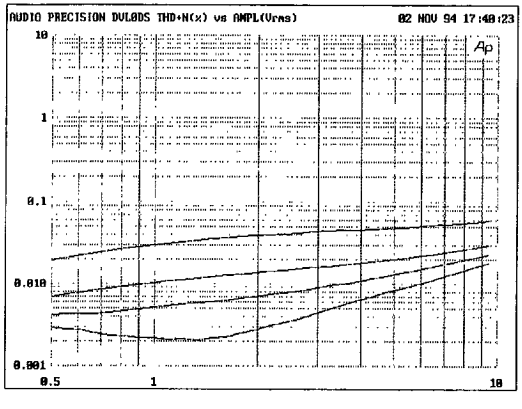

Figure 16. THD+N vs. Input Level at +15 dB Gain (see text).

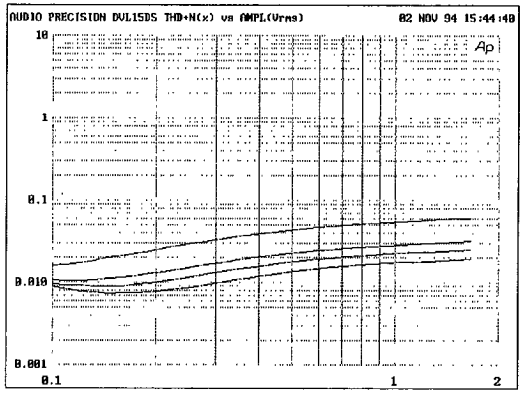

Figure 17. THD+N vs. Input Level at -15 dB Gain (see text).

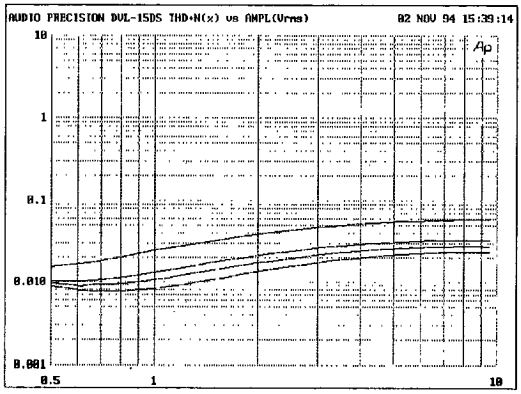

Figure 18. THD+N vs. Frequency at 0 dB gain (see text).

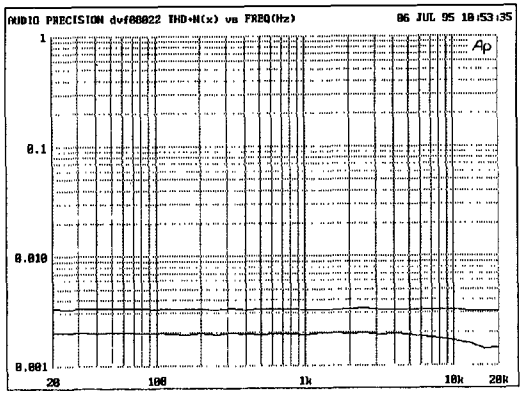

Figure 19. THD+N vs. Frequency at +15 dB Gain.

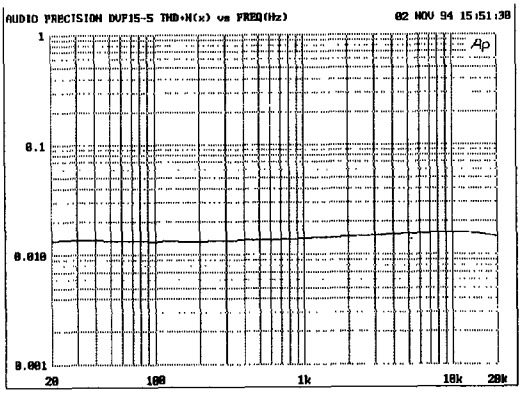

Figure 20. THD+N vs. Frequency at -15 dB Gain.

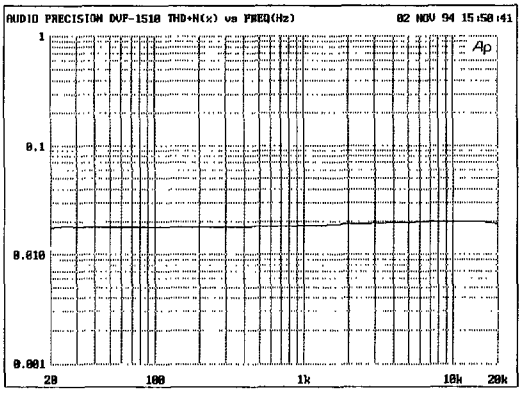

Figure 21. Output Offset vs. Gain Control Voltage (10 dB/volt) (see text).

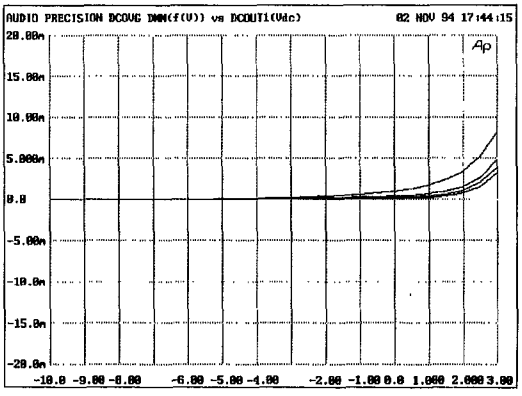

Figure 22. 22 kHz BW Noise vs. Gain Control Voltage (10 dB/volt)

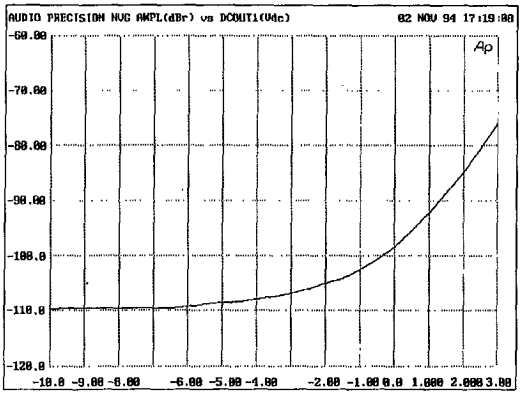

Figure 23. 22 kHz BW Noise vs. Input Level at 0 dB Gain (see text).

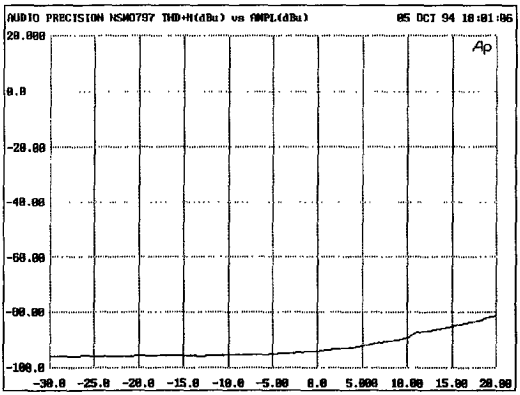

Figure 24. Same as Figure 23, but with TL081 Control Voltage Buffer (see text)