THAT Corporation

Low-Noise Matched Transistor Array Die

THAT 380G

FEATURES

- 4 Matched NPN and 4 Matched PNP
- Monolithic Construction
- Low Noise
  - 0.75 nV/ √Hz (PNP)
  - 0.8 nV/ √Hz (NPN)
- High Speed
  - f_T = 350 MHz (NPN)
  - f_T = 325 MHz (PNP)
- Excellent Matching – 500 µV typical between devices of same gender
- Dielectrically Isolated for low crosstalk, high DC isolation, and high temp operation
- 36V V_{CEO}

APPLICATIONS

- Microphone Preamplifiers
- Current Sources
- Current Mirrors
- Log/Antilog Amplifiers
- Multipliers
- Servos

Description

The THAT 380G is a large-geometry, 8-transistor, monolithic NPN/PNP array intended for use in multichip modules, hybrids, and chip-on-board applications. The individual devices exhibit both high speed and low noise, and are well-matched between transistors of the same gender.

Fabricated in a dielectrically isolated, complementary bipolar process, each transistor is electrically insulated from the others by a layer of insulating oxide (not the reverse-biased PN junctions used in conventional arrays) and exhibit inter-device crosstalk and DC isolation similar to that expected from discrete transistors. The resulting low collector-to-substrate capacitance produces a typical NPN f_T of 350MHz (325 MHz for the PNPs). Substrate biasing is not required for normal operation, though the substrate should be grounded to optimize speed and minimize crosstalk.

While not guaranteed to meet its datasheet specifications outside the commercial temperature range, the transistors on the 380G will typically operate at much higher temperatures than ordinary junction-isolated devices with similar packing density.

Quad transistor arrays in DIP and SO packages with similar performance characteristics are also available from THAT Corporation. Please contact us directly or through your local distributor for more information.

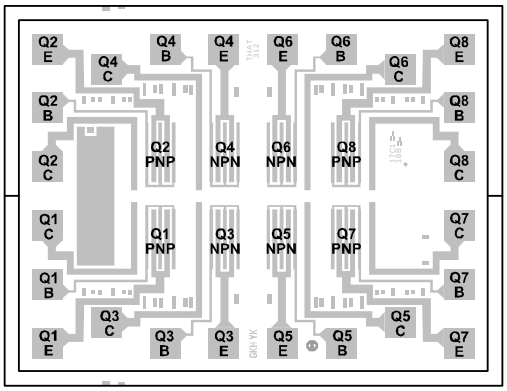

Figure 1. THAT 380G die layout

Die Thickness	Order Number
0.014”	380G14

Table 1. Ordering Information

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SPECIFICATIONS[1]

Absolute Maximum Ratings[2,3]

NPN Collector-Emitter Voltage (BV_{CEO})	36 V	Collector Current	30 mA
NPN Collector-Base Voltage (BV_{CBO})	36V	Emitter Current	30 mA
PNP Collector-Emitter Voltage (BV_{CEO})	–36 V	Operating Temperature Range (T_{OP})	-40 to +85 °C
PNP Collector-Base Voltage (BV_{CBO})	–36 V	Maximum Junction Temperature (T_{JMAX})	+125 °C
Collector-Substrate Voltage (BV_{CS})	± 100 V	Storage Temperature (T_{ST})	-45 to +125 °C

NPN Electrical Characteristics[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
NPN Current Gain	h_{fe}	V_{CB} = 10 V				
		I_C = 1 mA	60	100	—	
		I_C = 10 µA		100	—	
NPN Current Gain Matching	Δh_{fe}	V_{CB} = 10 V, I_C = 1 mA	—	5	—	%
NPN Noise Voltage Density	e_N	V_{CB} = 10 V, I_C = 1 mA, 1 kHz	—	0.8	—	nV√Hz
NPN Gain-Bandwidth Product	f_T	I_C = 1 mA, V_{CB} = 10 V		350		MHz
NPN ΔV_{BE} (V_{BE3}-V_{BE4} ;V_{BE5}-V_{BE6})	V_{OS}	I_C = 1 mA	—	±0.5	±3	mV
		I_C = 10 mA	—	±0.5		mV
NPN ΔI_B (I_{B3}-I_{B4}, I_{B5}-I_{B6})	I_{OS}	I_C = 1 mA	—	±500	±1500	nA
		I_C = 10 µA	—	±5		nA
NPN Collector-Base Leakage Current	I_{CBO}	V_{CB} = 25 V	—	25	—	pA
NPN Bulk Resistance	r_{BE}	V_{CB} = 0 V, 10 µA < I_C < 10 mA	—	2	—	Ω
NPN Base Spreading Resistance	r_{bb}	V_{CB} = 10 V, I_C = 1 mA	—	30	—	Ω
NPN Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1 mA, I_B = 100µA	—	0.05		V
NPN Output Capacitance	C_{OB}	V_{CB} = 10 V, I_E = 0 mA, 100 kHz		3		pF
NPN Breakdown Voltage	BV_{CEO}	I_C = 10 µAdc, I_B = 0	36	40	—	V
Input Capacitance	C_{EBO}	I_C = 0 mA, V_{EB} = 0 V	—	5	—	pF

PNP Electrical Characteristics[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
PNP Current Gain	h_{fe}	V_{CB} = 10 V				
		I_C = 1 mA	50	75	—	
		I_C = 10 µA		75	—	
PNP Current Gain Matching	Δh_{fe}	V_{CB} = 10 V, I_C = 1 mA	—	5	—	%
PNP Noise Voltage Density	e_N	V_{CB} = 10 V, I_C = 1 mA, 1 kHz	—	0.75	—	nV√Hz

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PNP Electrical Characteristics[2] (cont'd)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
PNP Gain-Bandwidth Product	f_T	I_C = 1 mA, V_{CB} = 10 V		325		MHz
PNP ΔV_{BE} (V_{BE1}-V_{BE2}; V_{BE7}-V_{BE8})	V_{OS}	I_C = 1 mA	—	±0.5	±3	mV
		I_C = 10 µA	—	±0.5		mV
PNP ΔI_B (I_{B1}-I_{B2}; I_{B7}-I_{B8})	I_{OS}	I_C = 1 mA	—	±700	±1800	nA
		I_C = 10 µA	—	±7		nA
PNP Collector-Base Leakage Current	I_{CBO}	V_{CB} = 25 V	—	–25	—	pA
PNP Bulk Resistance	r_{BE}	V_{CB} = 0 V, 10µA < I_C< 10 mA	—	2	—	Ω
PNP Base Spreading Resistance	r_{bb}	V_{CB} = 10 V, I_C = 1 mA	—	25	—	Ω
PNP Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1 mA, I_B = 100 µA	—	–0.05		V
PNP Output Capacitance	C_{OB}	V_{CB} = 10 V, I_E = 0 mA, 100 kHz		3		pF
PNP Breakdown Voltage	BV_{CEO}	I_C = -10 µAdc, I_B = 0	-36	-40	—	V
Input Capacitance	C_{EBO}	I_C = 0 mA, V_{EB} = 0 V	—	6	—	pF

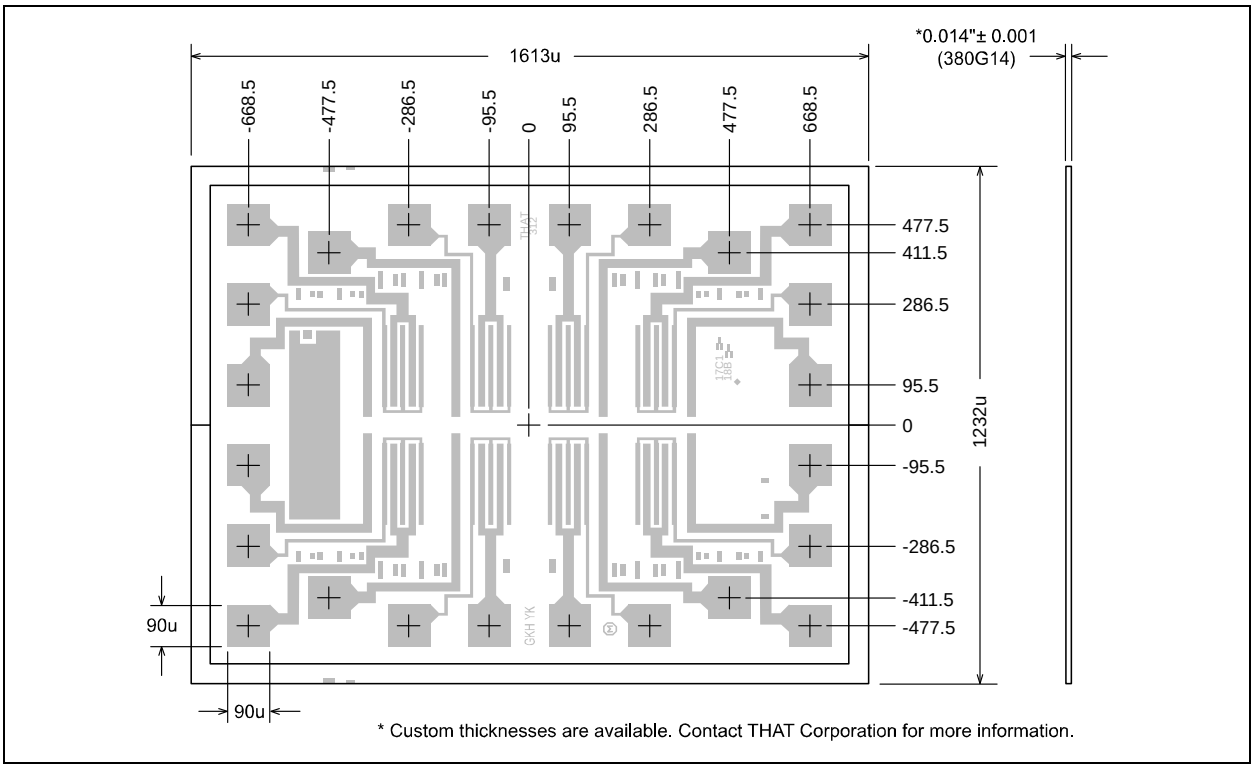

Figure 2. Die dimensions

1. All specifications are subject to change without notice.
2. Unless otherwise noted, T_A = 25ºC.
3. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rati ngs only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THAT Corporation believes all the information furnished in this data sheet is accurate and reliable. However we assume no responsibility for its use nor for any infringements of third-party intellectual property which may result from its use.

LIFE SUPPORT POLICY

THAT Corporation ICs are not designed for use in life support equipment where a malfunction of our ICs might reasonably result in injury or death. Customers who use or sell our ICs for such life suport application do so at their own risk, and shall hold THAT Corporation harmless from any and all claims, damages, suits, or expenses resulting from such use or sale.

CAUTION: THIS IS AN ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE

Electrostatic charges in the range of several kV can accumulate on the human body as well as test and assembly equipment. This device can be damaged by the currents generated by electrostatic discharge from bodies and equipment. Moreover, the transistors in this device are unprotected in order to maximize performance and flexibility. Accordingly, they are more sensitive to ESD damage than many other ICs which include protection devices at their inputs. Note that all of the pins are susceptible.

Use ESD-preventative measures when storing and handling this device. Unused devices should be stored in conductive packaging. Packaging should be discharged to the destination socket before the devices are removed from their packages. ESD damage can occur to these devices even after they are installed in a board-level assembly. Circuits should include specific and appropriate ESD protection.

Revision History

Revision	ECO	Date	Changes	Page
00	—	6/25/07	Release	
01	2393	4/13/10	Changed Max. Operating Temperature from "0 to 70 °C" to "-40 to 85 °C".	2
02	2776	4/30/13	-Revised Maximum Rating section -Added NPN Breakdown Voltage spec. -Added PNP Breakdown Voltage spec. -Revised disclaimer text	2 2 3 4
03	2884	7/10/14	-Removed the 0.021" thick version	13

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