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A Flexible Compander IC for Wireless Microphone Applications

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ABSTRACT

A new IC for implementing companding noise reduction in professional wireless microphone applications is described. Unlike existing devices designed primarily for the cordless telephone market, the new design allows straightforward, repeatable implementation of companding schemes incorporating ratios greater or less than 2 to 1, level-dependent ratios, limiters, and noise gates. The overall device architecture and design and performance of individual functional blocks is described. Several examples of encoder and decoder implementations are presented. The design techniques used to maintain wide dynamic range while minimizing power consumption are described.

1. INTRODUCTION

Contemporary analog wireless microphone systems almost universally employ companding noise reduction systems to circumvent the dynamic-range limitations of the FM transmission channel. Many existing designs employ compander ICs originally designed for application in cordless telephones. Such devices are internally configured for a fixed two-to-one compression ratio (and corresponding one-to-two expansion ratio). The audio performance of these ICs, particularly those that feature the lowest power consumption, often falls short of that desired for professional microphones.

This paper describes a new IC that provides the wireless microphone designer with the flexibility to implement a wide range of companding schemes tailored to the channel they will be used around, while maintaining high audio quality and low power consumption. The first section illustrates the overall architecture of the chip. In subsequent sections, the design and performance of each of the functional blocks is briefly described. Finally, it is shown how these blocks may be easily configured to form compressors and expanders with a wide range of ratios and repeatable characteristics that are insensitive to temperature or power-supply voltage, and that track one another over a very wide range of signal levels.

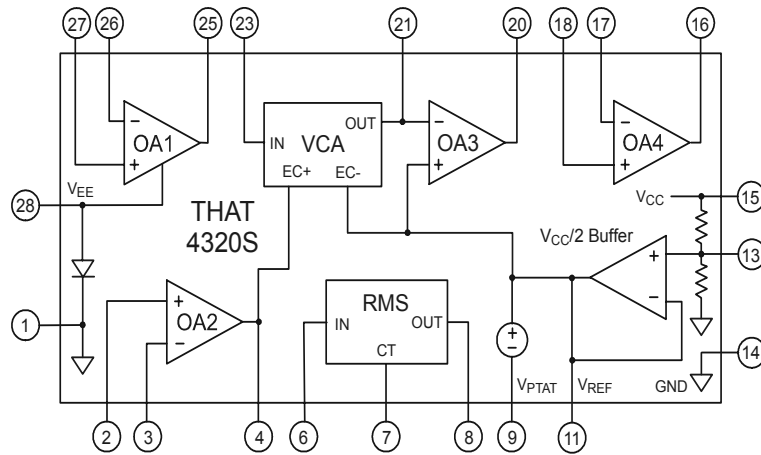


Figure 1: Componder IC Block Diagram

2. IC ARCHITECTURE

Figure 1 is an equivalent block diagram of the new integrated circuit. The functional blocks include an exponentially-controlled voltage-controlled amplifier (VCA), a logarithmic-output, true-RMS-level detector, a proportional-to-absolute-temperature (PTAT) voltage reference, a buffered mid-supply reference, and four operational amplifiers. The design and performance of each is briefly described below.

2.1 VCA

The VCA topology is substantially similar to that described in a previous paper [1]. The circuit accepts a current input via a virtual ground (at pin 23 in Figure 1), and delivers a current output into the virtual ground created by current-to-voltage converter opamp OA3 (at pin 21 in Figure 1). The VCA inherently has two opposing-polarity control ports, shown as E_{C+} and E_{C-} in Figure 1. The current gain of the VCA as a function of the voltage difference between the control ports is:

$$I_{out}/I_{in} = \exp(V_C/2V_T) \quad (1)$$

Where V_C is the voltage difference between the E_{C+} and E_{C-} control ports, and V_T is the “thermal voltage” kT/q . In the current design the voltage at the E_{C-} control port is held constant at a mid-supply reference voltage, while all gain control occurs via the E_{C+} control port.

If we define the VCA current gain in dB as:

$$dBgain = 20 \log(I_{OUT}/I_{IN}) \quad (2)$$

then, it follows that:

$$dBgain = 20 \log[\exp(V_C/2V_T)] \quad (3)$$

and, at room temperature of 300°K :

$$dBgain = \frac{10V_C}{V_T} \log(e) = V_C/(5.99 \text{ mV}) \quad (4)$$

Thus, the VCA gain is linear in dB with a 6 mV/dB scaling at room temperature.

Input voltages are converted to currents by an external impedance connected to pin 21. The maximum input and output currents that the VCA can accept are a function of an internal bias current. In the new design this bias current is made a function of the power-supply voltage such that signal handling capability is proportional to supply voltage. Thus, when the supply voltage is low, and, consequently, surrounding circuitry has less voltage excursion capability, the VCA standby current is reduced. This results in lower total power supply current for the IC, which is particularly appropriate in the case of a compressor in a battery-powered wireless microphone. When the supply voltage is higher, signal-current handling capability is increased, which is appropriate for the case of an expander in a line-powered wireless microphone receiver.

The gain-control range of the VCA exceeds 140 dB (from -90 dB to +50 dB). It is limited at the lower extreme by the onset of saturation in one or more of the gain-cell transistors. It is limited at the upper extreme by the gain-bandwidth product, which begins to roll off the upper end of the audio band at gains above 50 dB. In a typical application circuit with a +5 V power supply and 20-kohm resistors for input voltage-to-current conversion and output current-to-voltage conversion, distortion is typically less than .05% for signals up to just before the clip level of $3.5 V_{rms}$. At unity gain, with the same

application circuit, the output noise in a 22 Hz to 22 kHz bandwidth is -98 dBV, and varies with gain as described in reference [1].

2.2 RMS-Level Detector

The true-RMS-level detector is a logarithmic-output

$$V_{RMS} = -\frac{V_T}{\tau}t + 2V_T \ln\left(\sqrt{\frac{1}{\tau} \int \left(\frac{I_{IN}}{I_0}\right)^2 \exp\left(\frac{t}{\tau}\right) dt}\right),$$

where $\tau = \frac{V_T C_T}{I_0}$ (7)

Equation (7) shows that the voltage V_{RMS} is proportional to twice the logarithm of the exponentially time-weighted RMS level of the input current, Also,

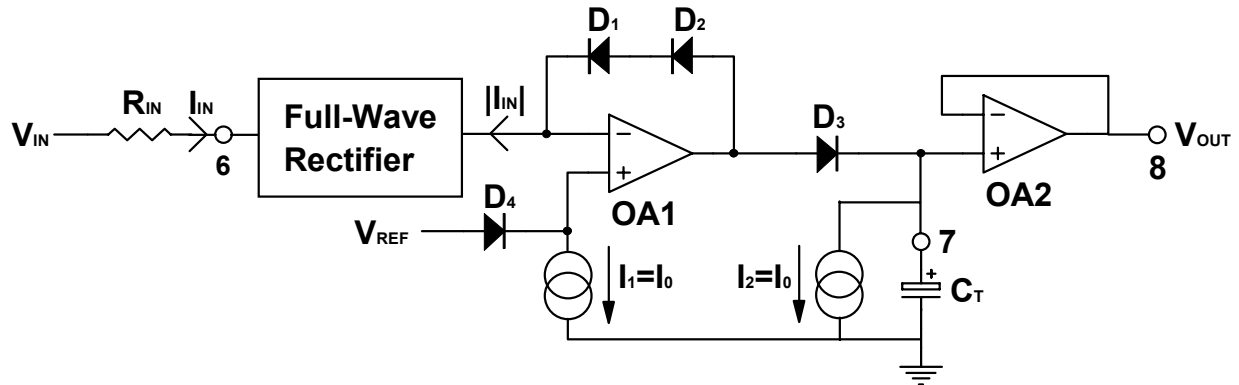


Figure 2: RMS-Level Detector Simplified Schematic

type using a log-domain filter to implement the averaging time constant. The theoretical operation is well-described mathematically in reference [2]. A simplified schematic of the topology is shown in Figure 2.

The circuit accepts an input current via a virtual ground (at pin 6 in Figure 2). The input current is full-wave rectified and the resulting output current is the logging circuit around OA1 in Figure 2. The voltage at the output of OA1 (with respect to V_{REF}) is:

$$V_{OA1} = 2V_T \ln\left(\frac{|I_{IN}|}{I_S}\right) - V_T \ln\left(\frac{I_0}{I_S}\right) \quad (5)$$

where I_{IN} is the input current to the detector, I_0 is an internal reference current, and I_S is the saturation current of diodes D_1 , D_2 , D_3 , and D_4 in Figure 2, which are all assumed to be identical. This may be rewritten:

$$V_{OA1} = V_T \ln\left(\frac{|I_{IN}|}{I_S}\right)^2 - V_T \ln\left(\frac{I_0}{I_S}\right) \quad (6)$$

Diode D_3 , current source I_2 , and external capacitor C_T form a log-domain filter. Such filters are a type of externally linear, internally nonlinear filters, that, “when placed between a log converter and an anti-log converter (exponentiator), will cause the system to act as a linear filter” [3]. Using the approach illustrated in reference [2], it may be shown that the voltage V_{RMS} at the cathode of log-filter diode D_3 (and at the output of buffer opamp OA_2) is:

when the steady-state RMS level of the input current is equal to the reference current I_0 , $V_{RMS} = 0$. It’s worth noting that the log filter behaves as a single-pole lowpass filter with a cutoff frequency of $f_c = 1/(2\pi\tau)$. Thus, the integration time constant of the detector may be set via the external capacitor C_T .

As also illustrated in reference [2], for steady-state input currents whose frequency components f_i all satisfy: $f_i \gg 1/(2\pi\tau)$, equation (7) may be further simplified to:

$$V_{RMS} = 2V_T \ln \sqrt{\left(\frac{I_{INRMS}}{I_0}\right)^2} = 2V_T \ln\left(\frac{I_{INRMS}}{I_0}\right) \quad (8)$$

where I_{INRMS} is the true-RMS value of the input current. In this case, the fundamental frequency of the input waveform is substantially greater than the cutoff frequency of the log filter, $(1/2\pi\tau)$, and, thus, ac ripple components are substantially attenuated, leaving a dc output.

As mentioned above, the reference current I_0 defines the input current for which the detector output is 0 V (the 0 dB reference). In the new design, the value of master current source that is mirrored to the current sources at the cathodes of D_3 and D_4 in Figure 2 are trimmed at wafer level such that the reference input current is within +/-1.3 dB of the nominal value of 7.5 uA. Care is taken to ensure that this current does not vary substantially with power-supply voltage

(typically less than +/-0.3% over a 5 V to 15 V range) and to be relatively constant with temperature (typically less than +/-0.5% from 0° to 80° C).

The detector linearity is typically better than +/-0.25 dB (guaranteed to be +/-0.5 dB) over a 40 dB input range centered around the reference level of 7.5 uA RMS. Linearity over the 74 dB input range from 200 nA RMS to 1 mA RMS is typically better than +/-1 dB. Bandwidth exceeds the audio range over this range of input levels.

If we define the dB value of the RMS level of the detector input current with respect to the reference current, I_0 , as:

$$dB_{RMS} = 20 \log\left(\frac{I_{INRMS}}{I_0}\right) \quad (9)$$

then, from equation (8), we may write:

$$dB_{RMS} = 20 \log\left[\exp\left(\frac{V_{RMS}}{2V_T}\right)\right] \quad (10)$$

and, at room temperature of 300° K:

$$dB_{RMS} = V_{RMS}/(5.99 \text{ mV}) \quad (11)$$

Thus, the VCA gain-control-port scaling and RMS-level detector output scaling are identical. Moreover, since they share the same silicon, they track extremely well over temperature.

Since the RMS-level detector is responsive to the total power in a waveform, it is independent of phase shifts in individual frequency components in the waveform (for frequencies well above the cutoff frequency of the integration filter.) This has advantages in wireless microphone compander applications, since phase shifts in the FM transmission channel will not cause mistracking of the expander.

2.3 PTAT Voltage Reference

As shown above, the RMS-level detector output scaling and the VCA control-port scaling both have terms proportional to absolute temperature arising from the “T” in $V_T = kT/q$. If the detector output is connected directly to the VCA control port, as it would be in a fixed-ratio compressor or expander, all is well, since the temperature coefficients will cancel. Often, however, it is desirable to introduce thresholds in the input-output transfer where the compression or expansion ratio changes as a function of level. Also, it is often desirable to offset the VCA gain with a dc voltage. In these cases, a source of dc voltage independent of the power-supply voltage, and with a

PTAT coefficient, allows implementation of these features in a temperature independent manner.

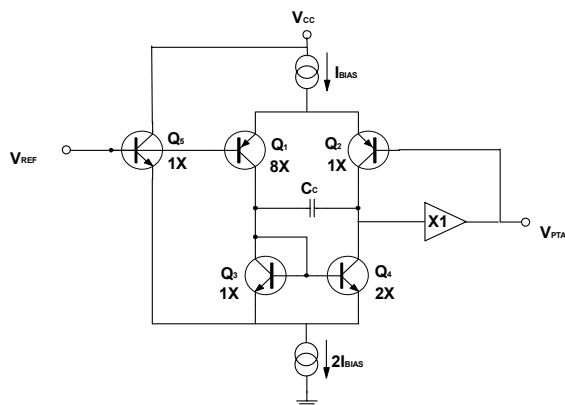


Figure 3: PTAT Generator Simplified Schematic

Figure 3 is a simplified schematic of the PTAT voltage reference in the new IC. The circuit buffers the mid-supply reference voltage, V_{REF} , and adds a PTAT offset of approximately -72 mV at room temperature. The 2-to-1 ratio in emitter areas of current-mirror transistors Q_3 and Q_4 force the collector currents of input transistors Q_1 and Q_2 to differ by a factor of 2. Thus, Q_1 , with 8X emitter area, has a collector current of $I_{BIAS}/3$, while Q_2 , with 1X emitter area has a collector current of $2I_{BIAS}/3$. By inspection:

$$V_{PTAT} = V_{REF} + V_{BE1} - V_{BE2} \quad (12)$$

where V_{BE1} and V_{BE2} are the base-emitter voltages of Q_1 and Q_2 , respectively. Therefore:

$$\begin{aligned} V_{PTAT} &= V_{REF} + V_T \ln\left(\frac{I_{BIAS}}{24I_S}\right) - V_T \ln\left(\frac{2I_{BIAS}}{3I_S}\right) \\ &= V_{REF} - V_T \ln(16) = V_{REF} - 72 \text{ mV} \end{aligned} \quad (13)$$

where I_S is the saturation current of Q_2 , and Q_1 is assumed to have a saturation current of $8I_S$. The nominal -72 mV (at 300° K) offset from V_{REF} has precisely the same PTAT temperature coefficient as the VCA control-port scaling and RMS-level detector output scaling, and tracks well since it originates from exactly the same source -- differences in base-emitter voltages of transistors on the same piece of silicon. It's worth noting (see equations (4) and (10)) that the value of V_{PTAT} represents -12 dB of VCA current gain or RMS-detector output voltage.

Transistor Q_5 in Figure 3 serves to keep the voltage across the $Q_1 - Q_4$ cell independent of supply voltage, assuring that the output voltage is as well. The input bias current of the output buffer is designed to be nominally $2I_{BIAS}/\beta_{NPN}$ to compensate for the I_{BIAS}/β_{NPN} supplied from the collector of Q_3 to the bases of Q_3 and Q_4 . Compensation capacitor C_c keeps the loop stable for capacitive loads up to 180 pF.

2.4 Mid-Supply V_{REF} Buffer

The new IC is designed primarily for single-supply applications (though dual supply use is not precluded), since this is the most common configuration in battery-powered wireless products. Hence, the chip contains a buffered mid-supply reference voltage to which all signals are referred. This is shown in Figure 1 as the “ $V_{cc}/2$ Buffer”, along with voltage divider between V_{cc} and ground which feeds its input. The input of the buffer is brought out to an external pin (pin 13 in Figure 1) to allow an external capacitor to be connected from this node to ground to filter out power supply noise and thermal noise from the 20 kohm divider resistors. The resulting output noise with a 22 uF filter capacitor is around 7 nV/ $\sqrt{\text{Hz}}$ over most of the audio bandwidth.

The buffer opamp is unconventional in that it is externally compensated by a load capacitance connected from its output (at pin 11 in Figure 1) to ground. This was done in recognition of the fact that these ICs will, in the case of a wireless microphone handset or belt pack, coexist with an FM transmitter in very close proximity. This is a particular concern with the VCA, which is a multiplier with two very sensitive gain-control ports (6 mV/dB, remember) that will multiply the audio signal. Since one of these control ports is tied directly to V_{REF} , robust RF bypassing of this node is desirable. In this design, a minimum 10 nF capacitive load is required on the output, providing frequency compensation and RF bypassing simultaneously, with no concern for opamp stability in driving capacitive loads. This approach ensures that the source impedance presented at the buffer output continues to decrease with increasing frequency, at least up to the capacitor's self-resonant frequency.

2.5 Control-Voltage Buffer Opamp

Opamp OA2 in Figure 1 is internally connected to the positive-sense control port of the VCA. It is intended to provide a low-impedance drive to the VCA control port, which is necessary for low distortion. For the reasons cited above, it is also externally compensated

via a load capacitance connected between its output (pin 4 in Figure 1) and ground. It's electrically identical to the V_{REF} buffer.

2.6 Low-Voltage-Noise Opamp

Opamp OA1 in Figure 1 is designed for relatively low input voltage noise, typically 4.5 nV/ $\sqrt{\text{Hz}}$. One of its intended applications is as the preamplifier for low-impedance sources such as dynamic microphone capsules. In a typical wireless microphone, the maximum dynamic range is set by this stage of amplification. The output of this preamp will be fed to the noise-reduction compressor, after which noise is of much less concern. For this reason, OA1 has its negative power supply terminal brought to a separate pin on the package (pin 28 in Figure 1). To maximize system dynamic range, a separate negative supply voltage may be connected to this pin, while the rest of the IC is powered from the positive supply only. Since OA1 consumes only about 600 uA of the IC's total supply current, a simple voltage inverter may be employed to create the low-current negative supply rail. This will more than double the available voltage swing capability at OA1's output, increasing the dynamic range by more than 6 dB. (Changing from a single +5 V power supply to +/-5 V supplies increases the maximum swing at OA1's output from +4 dBu to +11.75 dBu.) If OA1's output voltage is converted to a current and then compressed, this dynamic range can be preserved through the system.

OA1 is otherwise designed to be suitable for audio use, with a gain-bandwidth product of 13 MHz and a slew rate of 4 V/usec.

2.7 Other Opamps

Opamps OA3 and OA4 in Figure 1 are electrically identical general-purpose opamps. OA3 is internally connected for use as the current-to-voltage converter at the VCA output, with its inverting input connected to the VCA output, and its non-inverting input connected to V_{REF} .

OA4 is an uncommitted opamp available for sidechain or signal processing. Since these opamps have somewhat higher input voltage noise (10.5 nV/ $\sqrt{\text{Hz}}$) than OA1, but feature lower input current noise (0.3 pA/ $\sqrt{\text{Hz}}$ vs. 0.9 pA/ $\sqrt{\text{Hz}}$), OA4 is more suitable for use as a preamplifier for higher impedance sources such as passive electric guitar pickups.

OA3 and OA4 have typical gain-bandwidth products of 7.3 MHz and slew rates of 3.2 V/usec.

3. APPLICATIONS

The following sections illustrate some of the ways in which this new IC may be configured to implement noise-reduction compressors and expanders tailored to the requirements of the channel that they will be used around.

3.1 Fixed-Ratio Componder

The fixed-ratio wideband componder is likely the simplest approach to syllabic noise reduction. Fixed ratio componders with a 2:1 compression (and expansion) ratio are the type most existing componder ICs are pre-configured to implement. Using higher ratios than 2:1 can be advantageous, as they reduce the dynamic range of the compressed signal even further, resulting in more noise reduction, and, for wireless microphone applications, minimize the chance of overmodulation of the FM carrier. Of course, the higher the ratio, the greater the audible consequences of mistracking between the encoder and the decoder. It is in such applications that the predictable performance of the VCA and detector, over a wide dynamic range, are most important.

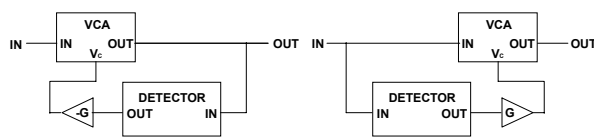


Figure 4: Componder Block Diagram

Figure 4 shows a block diagram of a simple feedback compressor and feedforward expander. For noise-reduction applications, the combination of a feedback compressor and feedforward expander is the most widely used topology. There are two primary reasons for this. The first is that, since we desire the two circuits to perform as mirror images of one another, it is important that the detectors see the same input signal, at least to the extent possible after any degradation by the transmission channel. The combination of a feedforward compressor and feedback expander could theoretically fulfill this requirement, but there is a second advantage that tips the balance in favor of the feedback compressor/feedforward expander combination. In this configuration both detectors monitor the compressed signal. This reduces the dynamic-range requirement of

the detectors and increases the chances of accurate tracking between the compressor and expander.

If the VCA and the Detector blocks in Figure 4 are assumed to behave as described above in sections 2.1 and 2.2, the analysis becomes quite straightforward. (This approach to analyzing log-based compressors and expanders is explored more fully in reference [4]).

Beginning with the compressor, if we express the input and output levels in decibels, in this case with respect to the reference input level of the RMS detector, we may write by inspection:

$$dB_{out} = dB_{in} + dB_{gain} \tag{14}$$

where dB_{gain} is the VCA gain in dB as in equation (4), dB_{out} is the output level in dB with respect to the detector reference level, and dB_{in} is the input level with respect to the detector reference level. Equation (14) merely states that the output signal is the input signal multiplied by the VCA gain. Since dB_{out} is the input level to the detector, using equation (11) we may write:

$$V_{RMS} = .006 * dB_{out} \tag{15}$$

and, from the block diagram:

$$V_C = -G * V_{RMS} = .006 * (-G) * dB_{out}. \tag{16}$$

Using equation (4):

$$dB_{out} = dB_{in} - (G * dB_{out}) \tag{17}$$

and, rearranging:

$$dB_{out} = dB_{in} \left(\frac{1}{1+G} \right). \tag{18}$$

Thus, when $dB_{in} = 0$ dB with respect to the detector's input reference level, $dB_{out} = 0$ dB. For every 1 dB change in dB_{in} , up or down, dB_{out} will change only by $1/(1+G)$ dB.

We may define the compression (or expansion) ratio:

$$R_{FB} = \frac{dB_{in}}{dB_{out}} = 1 + G. \tag{19}$$

Note that we have chosen the sign for the gain block between the detector and the VCA control port as negative. Thus, the circuit is a compressor for $G > 0$ (and $R_{FB} > 1$), an expander for $G < 0$ ($R_{FB} < 1$), and unity gain for $G = 0$. There is, of course, a singularity at $G = -1$ (an infinite expander).

The feedforward expander may be analyzed in a similar fashion, leading to:

$$dB_{out} = dB_{in}(1 + G) \tag{20}$$

non-inverting input to V_{REF} properly references the VCA control voltage to V_{REF} , while the chosen value of R_7 provides approximate compensation for dc errors due to OA2's input bias currents.

The connection of V_{PTAT} via R_8 provides some additional static gain. Remembering from equation (13) that, with respect to V_{REF} , V_{PTAT} is $-V_T \ln(16)$, the contribution from V_{PTAT} to the output of OA2 will be $0.5 * V_T \ln(16)$. Substituting this value into equation (1) yields a VCA gain of:

$$I_{out}/I_{in} = \exp(0.5V_T \ln 16/2V_T) = 2. \quad (24)$$

A simpler approach is to recognize that V_{PTAT} 's nominal value of -72 mV represents -12 dB at the VCA's control-port scaling of 6 mV/dB. Multiplying this by -0.5 via OA2 yields +6 dB of VCA gain.

Figure 6 shows the resulting input-output characteristic. Note that the level at which input and output are equal is -22.3 dBu (59.4 mVrms). This is 4 dB above the reference input level voltage of the detector (37.4 mVrms = -26.3 dBu) as a result of the 12 dB of gain added via the R_3/R_1 ratio and the PTAT contribution through R_8 . The 12 dB of additional gain in the signal path only moves the curve up by 4 dB due to the 3-to-1 ratio of the compressor.

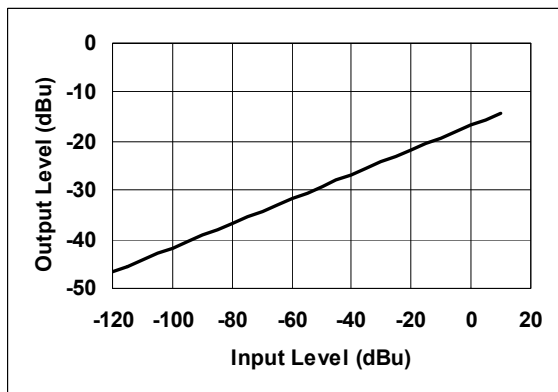


Figure 6: 3:1 Compressor Input-Output Characteristic

Also note that, for this simple compressor circuit, OA1 and OA4 are still available for use as preamplifiers or additional filtering.

Figure 7 shows the complementary feedforward 1:3 expander circuit, which may be analyzed in much the same way as the compressor circuit. Here OA2 sets G in from equation (21) to 2, resulting in a 1:3 expansion ratio. Components R_2 and C_2 have no effect on the signal path, but keep the high-frequency source impedance at the VCA input below 5 kohm, as is required for stability.

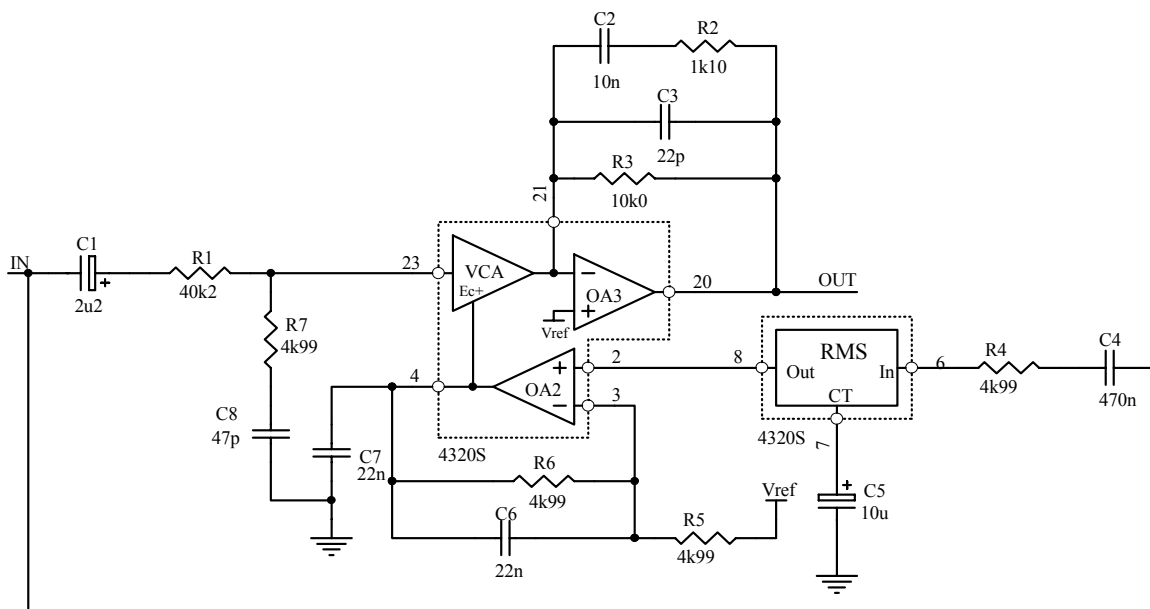


Figure 7: 3:1 Expander Schematic

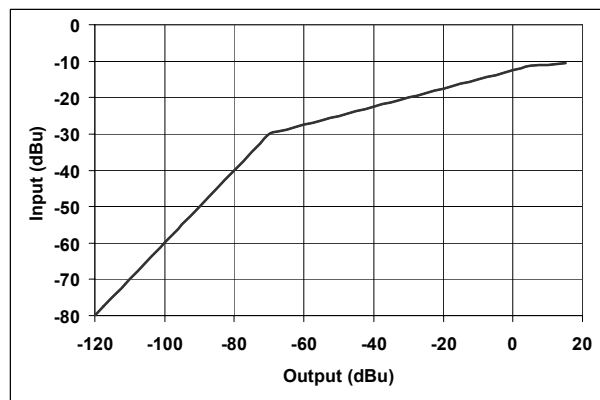


Figure 8: Level-Dependent Compressor Input-Output Characteristic

3.2 Componder with Level-Dependent Ratio

Compression and expansion ratios that vary with signal level can be advantageous in minimizing the audibility of compander operation. In particular, since low-level signals have little auditory masking potential, reducing the compression/expansion ratio to 1:1 for low-level

signals, which have little masking potential, can minimize the audibility of noise modulation [5].

Designers of wireless microphone products are also faced with increasingly strict regulatory strictures against overmodulation. Increasing the compression ratio to the “limiter” range (10:1 and above) at very high levels can provide a audible improvement over a simple clipper to limit modulation. If both techniques are employed, the clipper is activated only briefly until the limiter reduces the gain sufficiently.

The new IC provides the means to implement repeatable thresholds in the compression or expansion characteristic that are independent of power-supply voltage and temperature. An example of a compression input/output characteristic is shown in Figure 8. Beginning at the lowest input signal levels, we observe a 1:1 slope with a fixed 40 dB of signal gain. At an input level of -70 dBu, the characteristic transitions to a 4:1 compression slope. Above input level of +5 dBu, the compression slope increases to 16:1. Note that the input range from -110 dBu to +10 dBu is compressed to a total of about 60 dB (-70 dBu to -10 dBu).

Figure 9 shows a schematic for implementing this input-output characteristic using the new IC. The fixed

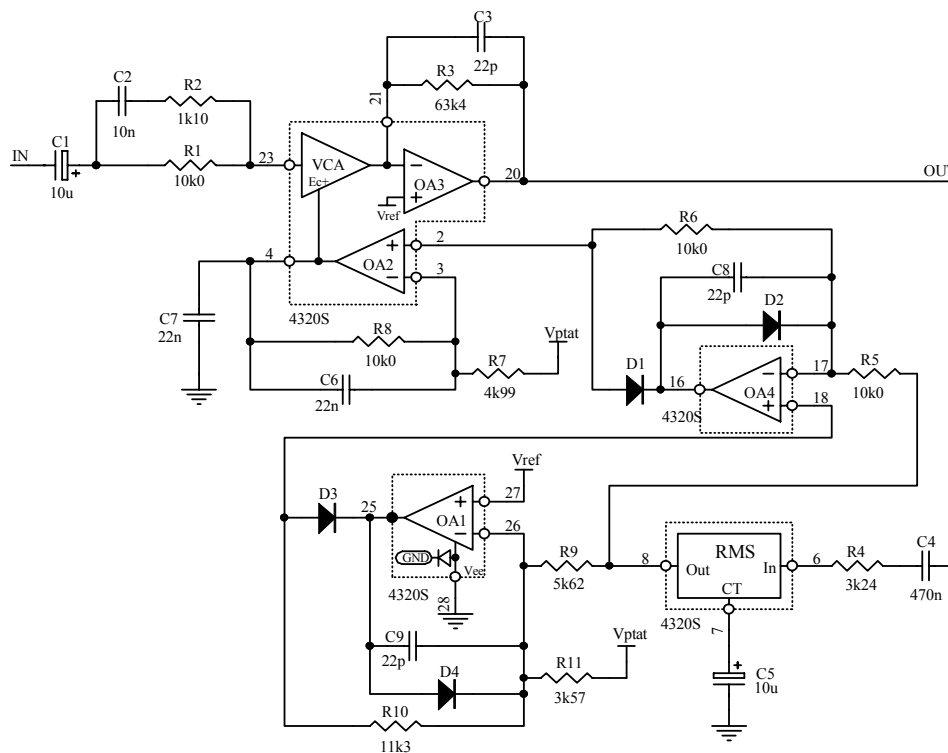


Figure 9: Level-Dependent Compressor Schematic

40 dB of gain at low input signal levels is accomplished through a combination of VCA current gain via the control port, and the ratio of input and output conversion impedances. The majority of the gain (+24 dB) is established by feeding V_{PTAT} to the VCA control port with a gain of -2 set by R_8 and R_7 . The other 16 dB is set by the ratio of R_3 to R_1 . (We are referring here to low-frequency gain. Gain at frequencies above 1 kHz is obviously increased by preemphasis network R_2/C_2 .)

The choice of how to establish the static gain (via the VCA control port or via impedance ratios) is somewhat arbitrary. However, there is a limit to how large R_3 can be made before the lowpass pole that it creates with C_3 begins to impair audio-band frequency response. C_3 is necessary to ensure stability by canceling the feedback pole formed by R_3 and the output capacitance of the VCA. As mentioned above in section 2.1, gain-bandwidth product limitations limit the useful audio-band VCA current gain to less than 50 dB.

The first threshold in the input/output curve occurs at an output level of -30 dBu, or 24.5 mVrms. Setting R_4 to 3.24 kohms results in an RMS detector reference input voltage of 24.3 mVrms. Therefore, the output of the detector will go from negative to positive as its input level moves through -30 dBu. OA3, along with D_1 , D_2 , R_5 , R_6 , and C_8 form an inverting half-wave rectifier that will pass only positive outputs from the detector to the non-inverting input of OA2, with a gain of -1. The net gain from the detector to the VCA control port via this path is -3, resulting in the desired 4:1 compression ratio.

The next threshold in the input/output curve occurs at an input level of +5 dBu, 75 dB above the first threshold. Referred to the output, this will be $(75 \text{ dB})/4 = 18.75 \text{ dB}$ above the -30 dBu output level of the first threshold, or -11.25 dBu. Thus, the half-wave rectifier formed by OA1, D_3 , D_4 , R_9 , R_{10} , and C_9 must begin to pass the detector's output to the non-inverting input of OA3 when it exceeds +18.75 dB. To accomplish this, R_{11} , connected to V_{PTAT} , must sink "18.75 dB" worth of current from OA1's summing junction. Recognizing that V_{PTAT} represents -12 dB worth of RMS-detector output voltage, we may write:

$$R_9/R_{11} = 18.75/12 = 1.56. \quad (25)$$

Choosing $R_9 = 5.62 \text{ kohms}$, $R_{11} = 3.57 \text{ kohms}$ satisfies this condition, and choosing $R_{10} = 11.3 \text{ kohms}$ sets the gain of this stage to -2 for signals that exceed the threshold. Thus, the net gain from the RMS-detector output to the VCA control port for output signals

above -11.25 dBu is -15, resulting in a compression ratio of 16:1.

Note that, though we have shown the internal low-noise opamp OA1 being used in the sidechain for this compressor, the characteristics enumerated in section 2.6 may make it more useful elsewhere in the audio signal path. A relatively inexpensive general-purpose opamp will serve nicely in the sidechain, since it is only required to handle slow-moving voltages with small excursions.

Figure 10 shows an example of a complementary expander input/output characteristic. Here, anticipating that line-powered receiver might have a higher available power-supply voltage, we have designed for a higher maximum output level. With a single +15 V supply, OA3 is capable of a +15.8 dBu output swing, so we have translated the input/output curve up by 10 dB, so that what was a +5 dBu input to the compressor becomes a +15 dBu output from the expander. We have also eliminated the second threshold, meaning that signals that were above the limit threshold will not be expanded back to their original level. In fact, the net result will be a 4:1 compression for signals above the limit threshold.

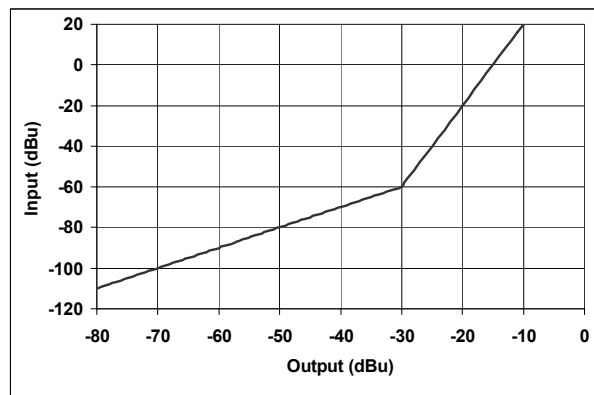


Figure 10: Level-Dependent Expander Characteristic

Figure 11 shows a schematic of a feedforward expander that implements the expansion characteristic. The 10 dB upward translation of the characteristic means that the static attenuation at low input levels need only be -30 dB, rather than the -40 dB that would

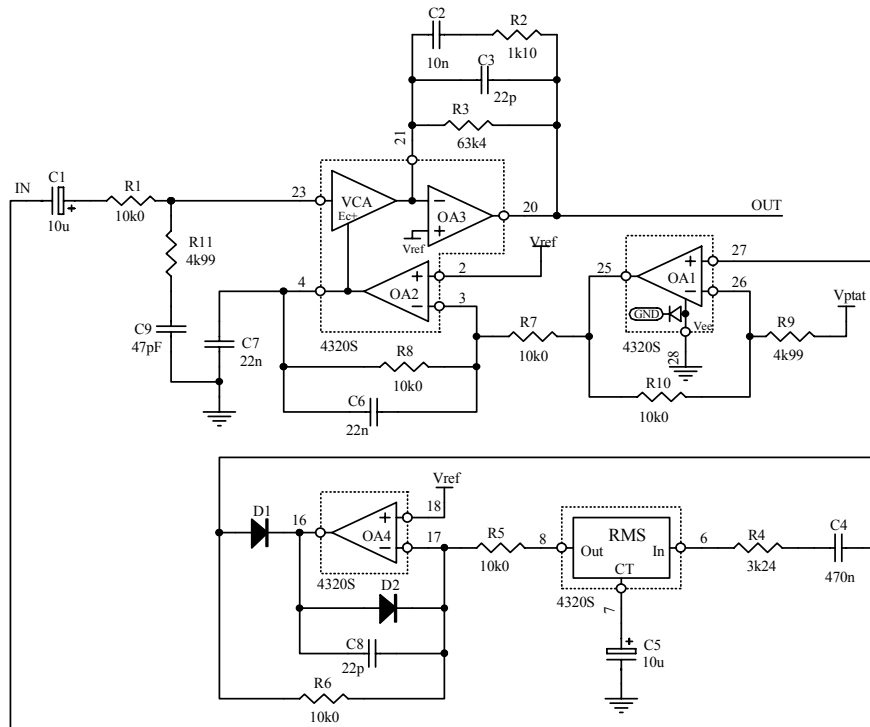


Figure 11: Level Dependent Expander Schematic

exactly complement the compressor characteristic. The ratio of R_3 to R_1 is set to produce -6 dB of low-frequency attenuation. The remaining -24 dB comes from the PTAT generator via OA1 and OA2 with a net gain of +2 to the VCA control port.

The RMS-level detector is again set up for an input reference level of -30 dBu, which is where the threshold occurs. The half-wave rectifier circuit around OA4 passes the detector output on to OA1 with a gain of -1 for input signal levels above this point. The net gain from the detector to the VCA control port in this case is +3, resulting in the 1:4 expansion ratio.

It is worth noting that, unlike the fixed-ratio compander, level mismatches between the output of the compressor and the input of the expander will result in mistracking in a level-dependent ratio compander. (In the fixed-ratio compander, they merely result in a static gain change.) However, for wireless microphone systems using FM transmission, maximum modulation levels from the transmitter must be controlled due to governmental regulations. At the receiver, the audio signal level resulting from a given modulation level can also be well-controlled, and is not subject to user adjustment. Thus, these systems can incorporate level-dependent ratio companders relatively easily.

4. SUMMARY AND CONCLUSIONS

The preceding circuits are intended solely as examples to demonstrate the flexibility and capability of the new integrated circuit. Since details such as the dynamic range and noise spectrum of transmission channels vary, compander circuitry should be designed with those characteristics in mind. The new IC gives designers the freedom to shape the compander circuit in many ways, while the consistency of the log-based signal processing ensures repeatable characteristics. As the IC consumes only 3.7 mA from a +5 V power supply, this performance does not come at the expense of battery life.

There are other approaches to compander circuitry that are possible with this IC that are beyond the scope of this paper. These include frequency dependent compression/expansion characteristics, multi-band companders, and level-dependent integration time constants for the RMS-level detector. Also, the thresholds in level-dependent compressors and expanders such as those described above, can easily be turned into “soft-knee” thresholds.

5. REFERENCES

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