AN IMPROVED MICROPHONE PREAMPLIFIER INTEGRATED CIRCUIT

FRED FLORU

THAT Corporation, Milford, MA, USA

The influence of the semiconductor process on the performance of a microphone preamplifier integrated circuit is described. Examples of active devices available in conventional junction isolated and newer complementary bipolar technologies are shown. The availability of such devices influences the electrical design and its complexity. The traditional microphone preamplifier topology is discussed. A new preamplifier gain structure, that extends the dynamic range by lowering the noise floor, is considered and its benefits are demonstrated.

0 INTRODUCTION

The dynamic range required by audio professional applications keeps getting larger and larger In order to keep up with the demand, the integrated circuits dedicated to such applications are manufactured in new and improved semiconductor processes. The dynamic range definition is the ratio between the maximum signal level that can be handled by the device and the noise floor. The maximum signal level that can be processed is for most designs a function of the maximum power supply voltage allowed by the device. Microphone preamplifiers, line receivers, line drivers, analog to digital and digital to analog converters (ADCs and DACs) are good examples of such applications where the limiting factors are the power supply rails [1] [2] [3] [4] [5]. For other device designs the maximum handled current is the limiting factor This category includes voltage controlled amplifiers and RMS (Root Mean Square) detectors [6] [7] [8]. Interestingly enough, the trend in the audio IC market for the maximum power supply voltage is going in both directions. Some manufacturers design parts that work at higher voltage supplies [1] [3] and others offer new devices that work at lower voltages [4] [5]. The lower power supply devices are manufactured in CMOS processes in which transistor sizes continue to shrink in order to allow higher density (and more digital functionality) at the expense of the device breakdown voltage.

1 FABRICATION PROCESS

The most common semiconductor processes for professional audio ICs are Junction Isolated (JI) bipolar, Dielectric Isolated (DI) bipolar and Complementary Metal Oxide Silicon (CMOS). There are no high quality preamplifiers made in CMOS process. CMOS is primarily used for ADCs, DACs and rail-to-rail operational amplifiers intended for low voltage applications. The technology of choice for microphone preamplifiers has been JI bipolar. The microphone preamplifier described in this paper is developed in a new complementary-bipolar DI process.

1.1 Junction Isolated Bipolar Process

Figure 1 shows a cross section of an NPN and lateral PNP transistor in JI process. The starting wafer material is of P-type on top of which a thin N-type epitaxial (also known as epi) layer is grown. Deep P-type isolation diffusions separate the N-type islands The heavily N-buried layer at the bottom of the island helps to reduce the collector series resistance The transistor base is formed by the P-type diffusion Finally, a heavily doped N-type diffusion inside the base creates the emitter region A similar heavily doped N-type diffusion outside the base, makes a good contact to the N-type epi layer for the collector terminal The current flow in the device is vertical, emitter through base and collected at the bottom by the N-buried layer. This structure makes good NPN transistors. The depth of the epi layer, minimum

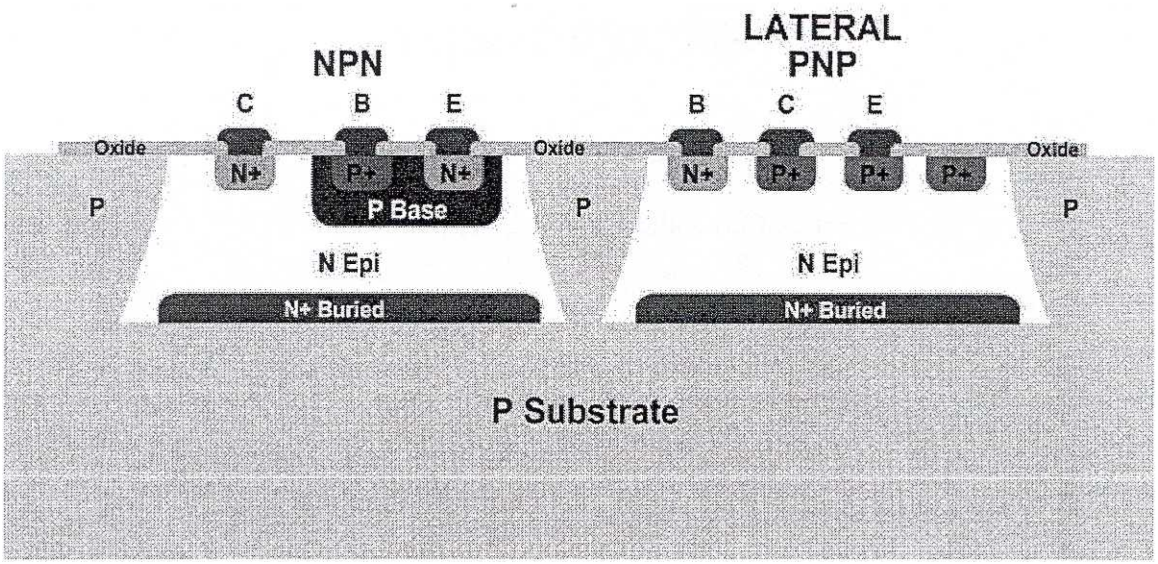

Figure 1. Bipolar transistors in Junction Isolated process

distances between collector contact and base diffusion, size and doping of the isolation P-type region define the maximum breakdown voltage of the device and ultimately the maximum power supply of the IC. Unfortunately, good PNP transistors are not available in this process. The only PNP devices available are either substrate PNPs and lateral PNPs. The substrate PNP uses the P-type wafer material as the collector. The base region is mostly the N-epi region and the emitter region is the P-type diffusion at the surface. The lateral PNP, shown in Figure 1, is formed by two closely located P-type diffusions, usually two concentric geometric shapes (circles, squares, etc.) The inner P-type diffusion is the emitter and the outer P-type diffusion is the collector. The N-epi in between forms the base The current flow in this transistor is horizontally at the surface Thus, the device performance is subject to surface imperfections None of these PNP transistors can match the performance of the vertical NPN The substrate PNP has a vertical current flow but the highly resistive N-epi region has negative effects in many electrical specifications. Also, the collector is always connected to the most negative power supply rail. The lateral PNP is difficult to control and usually has low current gain, also known as beta

Clever circuit design in JI process can overcome the shortage of good PNP devices up to a point The design is more complicated and it might take more silicon area as a result The P-type starting wafer has to be connected to the most negative power supply rail to maintain the isolation between the N-type tubs The isolation is provided by the carrier depleted region created by the reversed biased diode formed by the P-type substrate plus the isolation regions and the N-type tubs. The carrier depleted region at the p-n junction acts like a capacitor. The bigger the plates the more capacitance there is. Therefore, the larger the tub size, the greater the stray capacitance to substrate is On the bright side, the JI process is simple and inexpensive. It requires seven to eight mask sets. In other words it is a low cost process and well established.

Stray capacitance to the substrate could be a limiting factor for microphone preamplifiers in particular. The input transistors need to be large in order to have good noise performance The stray capacitance in the collector limits the maximum bandwidth achieved. To prevent this behavior, fairly low impedance is used in the collector of the input transistors that also have the effect of reducing the gain of the front-end At least a second amplification stage is required to make up for the lost gain. The output stage is also affected by the capacitance to the substrate The output transistors have considerable sizes to be able to handle the output current usually in the tens of milliampere The stray capacitance lowers the frequency bandwidth of these transistors as well

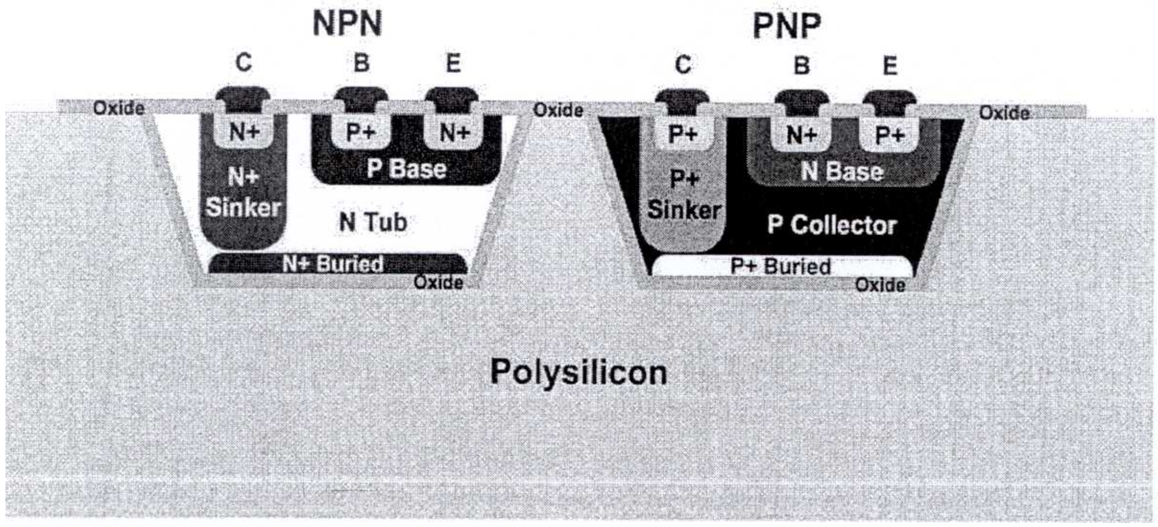

Figure 2. Bipolar transistors in Dielectric Isolated process

A major improvement in the quality of the JI bipolar process was made with the development of the complementary junction isolated bipolar process. It is more complex, it requires a few more masks and dual epitaxial layer growth [9]. It solved the problem of low performance PNP transistors. The idea is to create a P-type tub in an existing N-type tub. The PNP transistor is isolated by the reversed biased p-n junction between the two tubs Although performant, the PNP transistors have the same limitations of the NPN transistors, that is stray capacitance to power supply rails The electrical design in this process is a little bit simpler but the bandwidth of the device is limited.

The maximum power supply voltage that can be applied to an IC made in this technology is, among other factors, dependent on the isolation diode breakdown voltage The size of the isolation region is one of the differentiating factors between JI and DI processes. The breakdown voltage can be improved by increasing the size of the isolations between tubs. The tubs themselves have to increase in size to accommodate greater depletion regions due to high reversed voltages. The size of the die and the limiting factor that the stray capacitance has on the device performance limits the maximum practical breakdown voltage.

1.2 Dielectric Isolated Process

Figure 2 shows a cross section of an NPN and a PNP transistor. The starting material is an N-type wafer PNP tubs are produced by implanting a dose of P-type dopant and diffusing it into the N-type wafer. Each tub, N or P type, is defined using an isolation mask. The rest of the wafer, bare silicon, is etched away at a precise angle leaving V-shaped grooves in between the future tubs. Then the entire wafer is coated with a high quality oxide layer that can withstand hundreds of volts. A thick layer of polysilicon is then deposited on the wafer. It fills up the V-shaped grooves and creates a new wafer handle. The entire sandwich is turned upside down and the starting N-type wafer is ground away until the tubs are electrically separated by the layer of oxide and deposited polysilicon. Thus, the polysilicon can be either undoped, therefore a supplementary good insulator, or doped P or N type, therefore a good conductor. From this point on, the rest of the process is similar to JI process. Base and emitters are diffused in the same manner. To help lower the equivalent collector series resistor, an extra sinker step can be added. The sinker creates a low resistance path from the bottom of the tub (N-buried layer) to the contact area at the surface of the device.

Good quality vertical NPN and PNP transistors are readily available in DI process. This feature eliminates the need for lateral PNP devices. They can be made as well, but because of poor performance they are not often used Substrate transistors do not exist in this process because they are isolated from substrate by the high quality oxide.

The tubs are separated by oxide layers and the distance between them is not a limiting factor for the

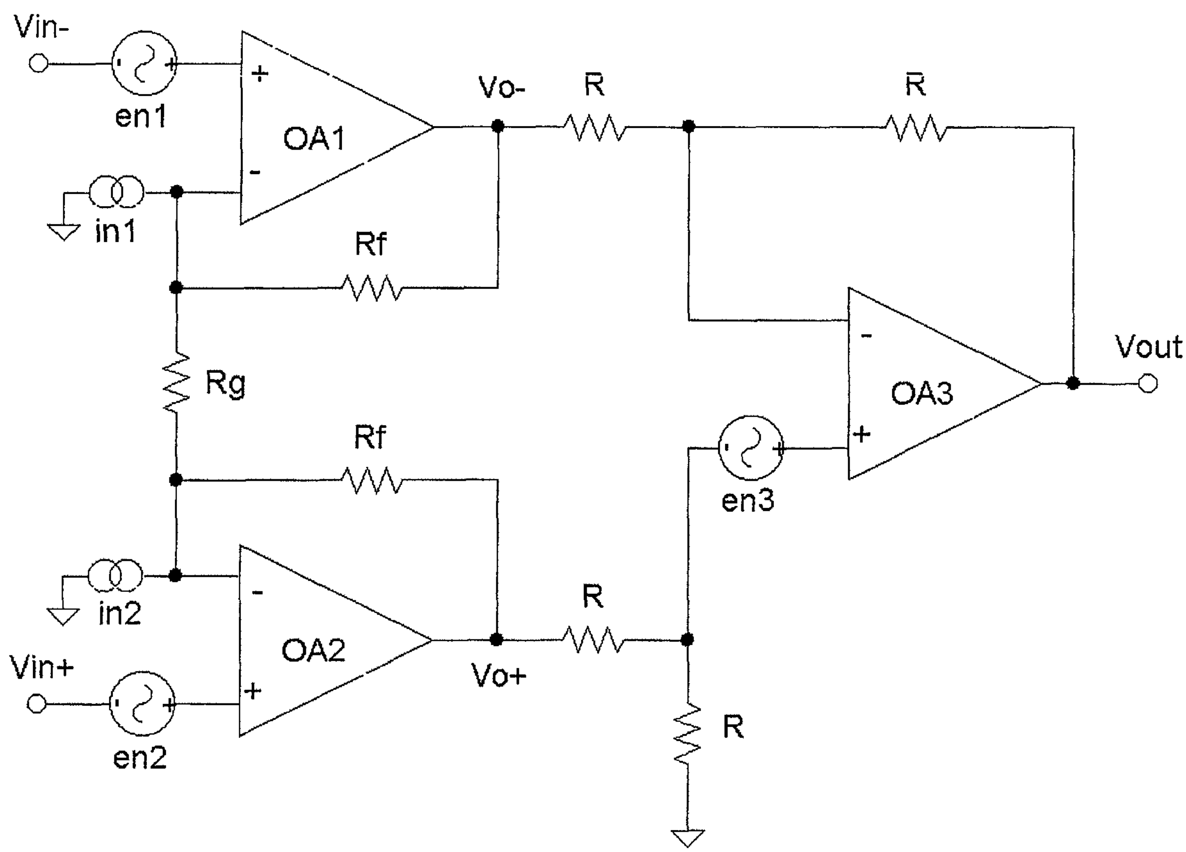

Figure 3 Traditional microphone preamplifier gain scheme

maximum power supply voltage (up to a few hundred volts.) This feature allows the tubs to be located much closer and it results in tremendous area savings up to 50%. Also, there is no reversed p-n junction anymore to isolate the tubs. As a result, the stray capacitance between the tub and the substrate is eliminated. This helps in designing large low noise transistors with high frequency bandwidth. Obviously, the small transistors have also reduced stray capacitance to substrate compared to JI process. This is the main reason why this process is mainly used for high frequency devices such as high performance video operational amplifiers Increasing the maximum power supply voltage in this process is a matter of sizing the tubs and tıansistors accordingly However the distance between the tubs is pretty much the same Therefore, it is not unheard of DI chips that have 400V poweı supply

The lack of stıay capacitance to the substrate makes the electrical design simpler. High gain can be achieved ıight at the front end ıesulting in lower number of total components. Another benefit is wide bandwidth at high gains. JI microphone preamplifiers have 100MHz to 200MHz gain bandwidth products at 60 dB of gain. It sounds like a lot but it means only 100kHz to 200kHz "-3dB" bandwidth at high gain settings DI microphone preamplifiers have between 1.5GHz to 3GHz gain bandwidth product at 60 dB of gain or 1.5MHz to 3MHz "-3dB" bandwidth at high gain settings. The difference is one order of magnitude. The bandwidth performance is important for high frequency Total Harmonic Distortion or THD performance. Typical low bandwidth amplifiers show an increase in THD with frequency.

The drawback of the DI pıocess is that it requires many steps and as a result can be expensive. Careful process design and die area savings can significantly ıeduce the overall cost.

2 SYSTEM DESIGN

2.1 Traditional

2.1.1 Topology

The traditional microphone preamplifier architecture is based on the three operational amplifier instrumentation amplifier. The front end consists of a differential amplifier with an external gain resistor. The output of the front end is converted from differential to a single ended by a unity gain difference amplifier. The front end has differential gain set by the external resistor and the common mode (CM) gain is always unity. Thus, the front end amplifier provides gain and the difference amplifier rejects the CM signals. All the available professional microphone preamplifiers ICs have a block diagram similar to the one shown in Figure 3.

The front end amplifier is made of operational amplifiers OA1 and OA2 and the two internal resistors labeled Rf. An external gain resistor Rg sets the gain. The difference amplifier consists of operational amplifier OA3 and four identical resistors R. The gain of the difference amplifier is one. Thus, the overall gain of the microphone preamplifier is as follows·

$$G = \frac{V_{OUT}}{(V_{in+} - V_{in-})} = 1 + \frac{2 \cdot Rf}{Rg} \qquad (1)$$

2.1.2 Choice of Resistor Material

In order to maintain the gain stable over temperature and time both Rf and Rg resistors must be low temperature coefficient and stable. Most of the resistors readily available in any bipolar semiconductor process, such as base resistors, emitter resistors or implant resistors have temperature coefficients in the order of thousands of parts per million (PPM) per degree Celsius (C) Also, the absolute values vary in a +/- 20% range. To make things worse, none of the diffusion resistors can be directly trimmed

The common choice for internal resistors Rf and R is a sputtered thin film. In this family, there are three major choices: TaNi, NiCr and SiCr. TaNi and NiCr have low sheet resistance up to 500 Ω/square TaNi is suitable for non passivated devices and laser trim because it self passivates when laser cut SiCr has high sheet resistance, usually from 500 Ω/square to 2 kΩ/square Thus, if the design has most of the resistors in the kΩ range, the resulting die is smaller. Although the resistor formula seems simple, a mix of two materials, additional ingredients make the resistor stable and with low temperature coefficients. The additional ingredients vary from manufacturer to manufacturer and they are usually a trade secret. Semiconductor manufacturers use the type that they developed and characterized as being stable over time Thin film materials are deposited in the same manner as metal on top of the wafer surface in a sputter machine.

The choices for resistor trimming are: laser trim, link blow and Zener zap. Laser trim is very efficient in terms of die area and achieves the best resolution. It can be set to linearly cut a resistor tab or blow thin film or metal links. Metal link blow could be achieved with another technique where a high current is injected into a thin piece of metal and eventually it opens the circuit. Zener zap design has resistors isolated by Zener diodes. A high current through the diode shorts it and connects parts of the circuit. The last two techniques require extra resistors and multiple pads increasing the die area.

2.1.3 Operational Amplifier Design

Traditionally in instrumentation amplifiers, operational amplifiers OA1 and OA2 are voltage feedback amplifiers (VFA). Microphone preamplifiers and high frequency instrumentation amplifiers use yet another option that is current feedback amplifiers (CFA). The block diagram of a simple example of VFA is shown in Figure 4. The base of transistor Q1 is the non-inverting input and the base of transistor Q2 is the inverting input. To a first approximation, the noise of this amplifier at high gains is due to transistors Q1, Q2 and half of resistor Rg. Figure 5 shows a simplified version of a CFA. The base of transistor Q1 is the non-inverting input and the emitter of Q1 is the inverting input. In this case the noise contribution at high gains is due to transistor Q1 and half of resistor Rg. It is obvious that in order to achieve the same noise performance the CFA takes less area and burns less power. Otherwise, in the case of VFA, to match the same performance as CFA, transistors Q1 and Q2 need to be much bigger. Also, to achieve low noise performance, the collector current of these transistors is in the milliampere range, therefore not trivial Consequently, a low noise VFA requires almost twice as much power.

Of course the VFA has its advantages The DC performance is much better and both inputs exhibit high impedance. In the case of the CFA, the DC performance is not that great In fact the inverting input is sitting at about -0.7V and has low input impedance. The output is also at about -0 7V. It can be set to about zero volts by injecting extra current into resistor Rf but the resulting offset is not going to match

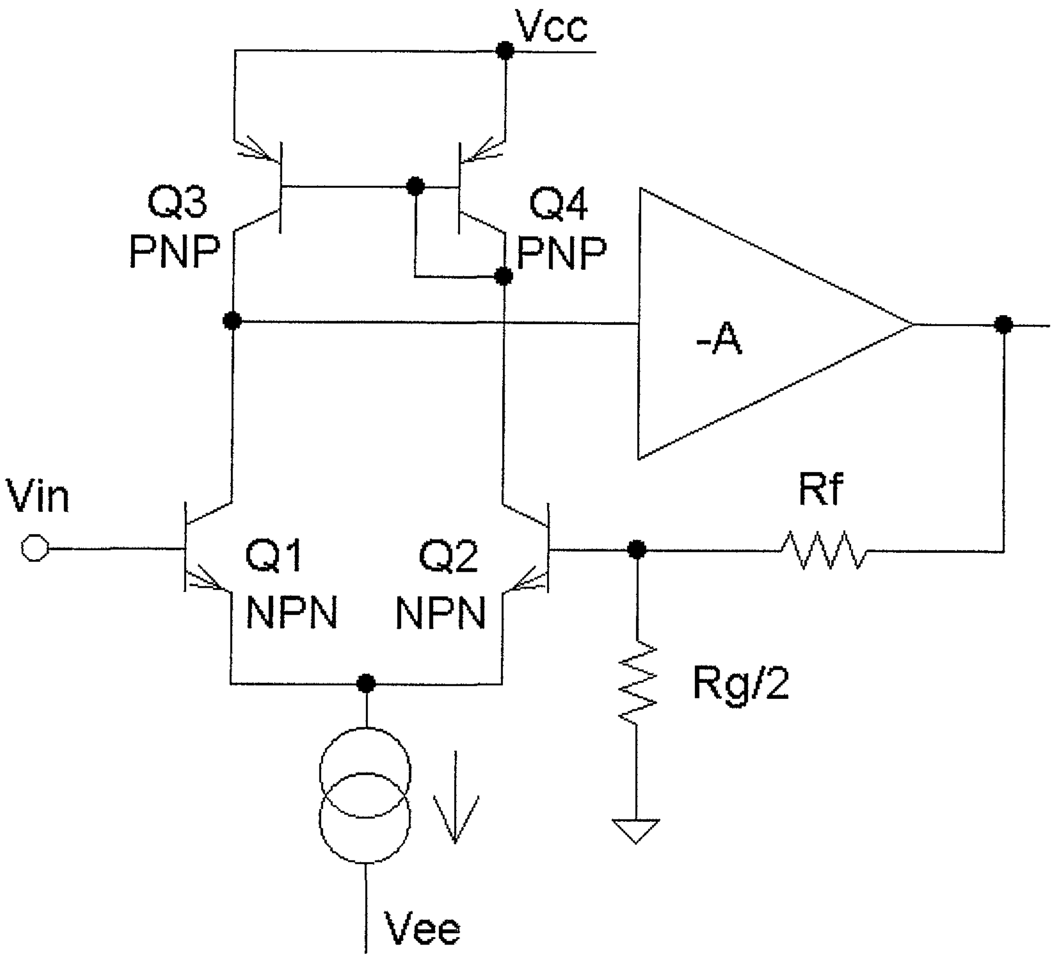

Figure 4. Voltage feedback operational amplifier.

the VFA performance Fortunately, the DC performance of a microphone preamplifier is not crucial.

The operational amplifier used in the difference block is of VFA type. Both inputs need to be high impedance and the operational amplifier has to have good common mode rejection. The noise of OA3 is not critical, at least at high gains. Usually the resistors around OA3 generate enough thermal noise to mask the noise of the amplifier. The resistor netwoık around OA3 is usually made of 5 to 6 kΩ resistors. A network of 5 kΩ has an equivalent noise, at OA3's input, of about 9 nV/√Hz . Thus, a 4 to 5 nV/√Hz operational amplifier is adequate for the job

2.1.4 Amplifier Dynamics

The maximum differential input voltage is limited by two factors: the maximum voltage that can be applied to each input and the maximum current available to drive the external gain resistor Rg. The maximum differential input voltage is dependent on the front end topology. The JI process topology is usually two cascaded NPN differential pairs sometimes combined with a folded cascode as shown in Figure 6a [2] This scheme lowers the maximum swing toward the positive rail. A folded cascode front end design, Figure 6b, achieves good swing toward the collector of the input transistor power rail For the other polaıity, the maximum swing is a function of the current source design The folded cascode requires good PNP tıansistors Therefore, it is a good choice for

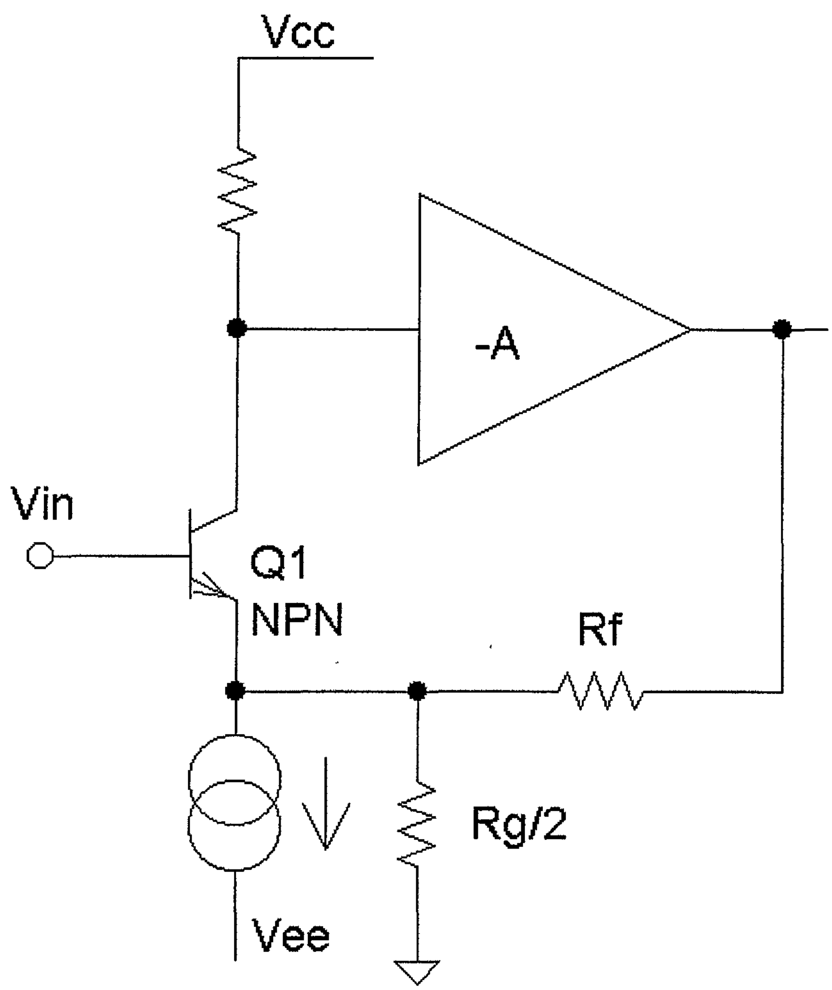

Figure 5. Current feedback operational amplifier.

complementary bipolar processes. The frequency compensation networks were omitted from Figure 6.

The current in the gain resistor Rg is supplied by the operational amplifiers OA1 and OA2. Since the differential input voltage appears across Rg, the current in this resistor is the input voltage divided by Rg. OA1 and OA2 should be able to provide the necessary current in order to obtain the maximum output voltage swing. Usually this current is in the 4 to 8 milliampere

The gain of the difference amplifier is one Therefore, the differential voltage applied at the input (V_{O+} - V_{O-}), as shown in Figure 3, can not be more than the maximum output voltage (the maximum peak output voltage is usually two - three volts less than the power supply rail). Thus:

$$V_{out} = (V_{O+} - V_{O-}) \tag{2}$$

If $|V_{O+}| = (-|V_{O-}|)$ then

$$V_{O+} = \frac{V_{out}}{2} \tag{3}$$

Each output of the front end amplifier V_{O+}, V_{O-}, has to swing only half of the maximum output voltage Under normal operating conditions the output of the front end amplifier never clips

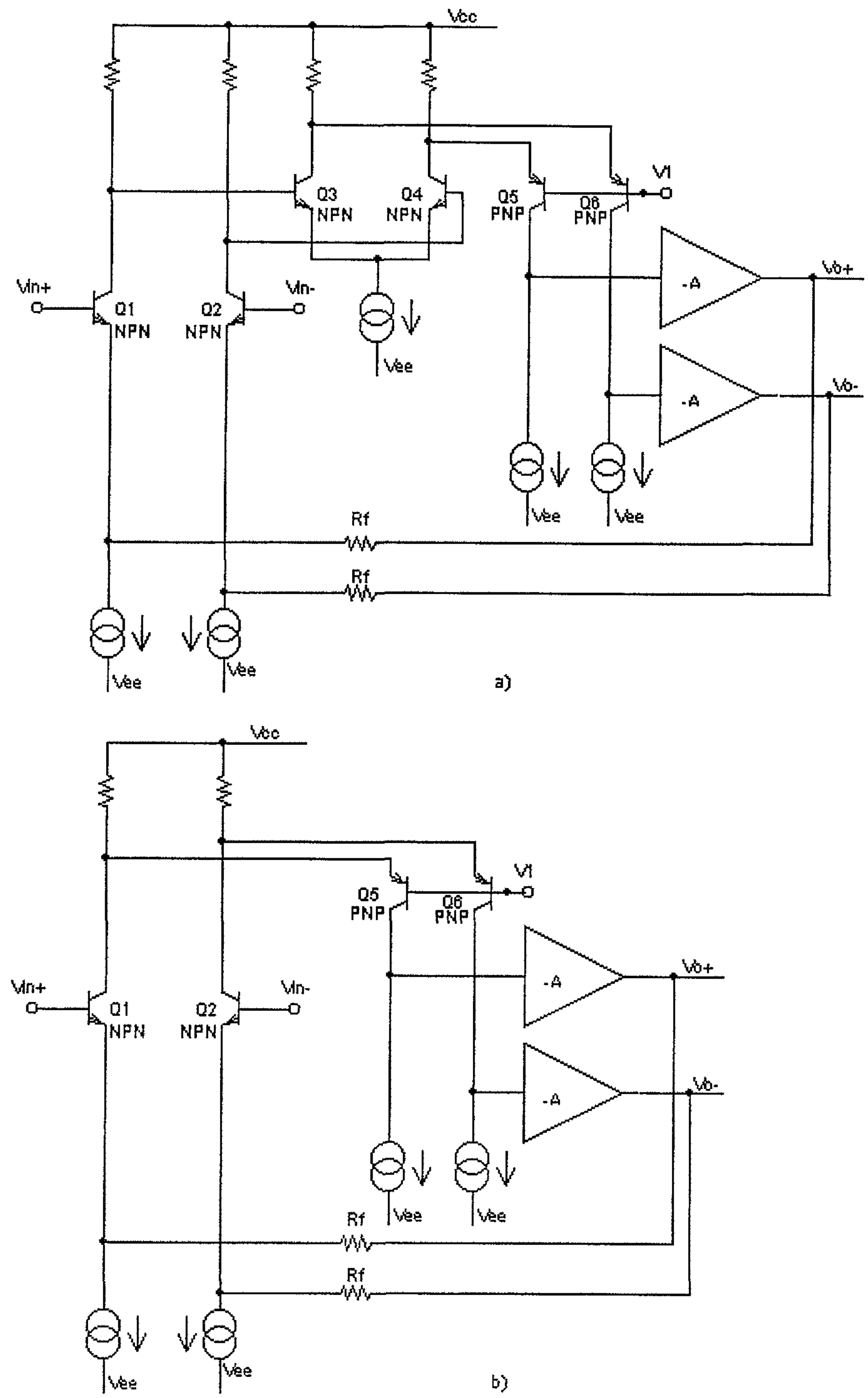

Figure 6. a) Typical front end operational amplifier in JI process
b) Front end operational amplifier in DI process

2.2 New and improved architecture

2.2.1 Topology

The new microphone preamplifier architecture is shown in Figure 7. It looks very similar to the traditional scheme in Figure 3. The main dissimilarity is the gain of the difference amplifier that in this case is half. The overall gain equation can be calculated from the following two gain equations:

$$V_{out} = \frac{1}{2} \cdot (V_{O+} - V_{O-}) \qquad (4)$$

$$(V_{O+} - V_{O-}) = (V_{in+} - V_{in-}) \cdot \left(1 + \frac{2 \cdot Rf}{Rg}\right) \qquad (5)$$

The preamplifier gain is calculated by substituting equation (5) into equation (4) as follows:

$$G_{new} = \frac{V_{out}}{(V_{in+} - V_{in-})} = \frac{1}{2} + \frac{Rf}{Rg} \qquad (6)$$

2.2.2 Differences between traditional and improved topologies

Microphone preamplifiers ICs based on traditional and new topology can not be directly interchanged because the gain equation is different at low gains. For instance, unity gain requires no Rg resistor in the traditional case and a 10 kΩ resistor in the new topology. If a potentiometer is used to control the preamplifier gain, unity gain is impossible with the old topology, as demonstrated by equation (1.) For 20 dB of gain, the traditional preamplifier requires a 1.1 kΩ resistor and the new configuration 526 Ω . At the other end of the gain spectrum, at 60 dB the traditional preamplifier calls for 10 Ω and the new one only 5 Ω. In a nut shell, if a traditional preamplifier is upgraded to the new architecture and the gain element(s) are left in place, there is a difference of approximately -6 dB in the overall gain.

The main benefit of the new architecture is extended dynamic range at lower gains. As stated in a previous chapter, the dynamic range is the difference between the maximum output signal level and the noise floor. For a given power supply, the maximum output signal level is the same for both configurations. The improvement comes in the noise floor. The new architecture adds another 5 to 10 dB to the dynamic range at unity gain, 4 to 8 dB at 20 dB of gain and 1.5 to 3 dB at 40 dB of gain. The performance at higher gains is similar.

To demonstrate the dynamic range improvement, a noise analysis is performed for both configurations. Let's assume that the equivalent input noise of the operational amplifiers OA1, OA2 and OA3 is e_{n1}, e_{n2} and e_{n3} , respectively. The equivalent input current noise sources are i_{n1} and i_{n2} for OA1 and OA2, respectively. OA3 has an equivalent input current noise source as welll, but it's usually less significant in the overall noise contribution. Therefore, is omitted from the Figure 3 and 4. OA1 and OA2 are similar and it's expected that the noise performance to be similar. Thus, we can assume that $e_{n1} = e_{n2}$ and $i_{n1} = i_{n2}$. However, note that although e_{n1} and e_{n2} are equal in value they are not correlated noise sources. The same is true for the current noise sources i_{n1} and i_{n2} . The contribution of each source at the output of the device is depicted as follows:

Voltage noise generated by OA1 and OA2:

$$\left[e_{n1}^2 \cdot \left(1 + \frac{2 \cdot Rf}{Rg}\right)^2\right] \cdot 2 \qquad (7)$$

The equivalent voltage noise of OA1 or OA2 is multiplied by the gain of the front end amplifier. The noise comes from OA1 and OA2, non correlated noise sources, therefore the multiplication by two at the end of the equation. Then, this noise component is multiplied by the gain of the difference amplifier which in this case is unity and it is not shown in the equation (7). By substituting gain equation (1) in to (7) the noise can be calculated as follows:

$$\left[e_{n1}^2 \cdot G^2\right] \cdot 2 \qquad (8)$$

Noise generated by the gain resistors in the front end amplifier:

$$\left\{\left[4 \cdot k \cdot T \cdot \left(Rf \| \frac{Rg}{2}\right)\right] \cdot \left(1 + \frac{2 \cdot Rf}{Rg}\right)^2\right\} \cdot 2 \qquad (9)$$

The thermal noise of a resistor is 4kTR where k is Boltzmann's constant 1.38 X 10^{-23} Joules/Kelvin [10], T is the temperature in Kelvin degrees (300 K at room temperature) and R the resistor value in ohms. In our case the equivalent resistor value is the parallel connection of Rf and half of Rg. The noise of the equivalent resistor is amplified by the front end gain. The multiplication factor by two is due to the fact that there are two such resistor networks in the front end circuitry. One around OA1 and one around OA2. Again, the difference amplifier gain does not show up in the equation because it is unity. The equivalent resistor in equation (9) can be rearranged as follows:

$$Rf \| \frac{Rg}{2} = \frac{Rf \cdot \frac{Rg}{2}}{Rf + \frac{Rg}{2}} = \frac{Rf}{1 + \frac{2 \cdot Rf}{Rg}} \qquad (10)$$

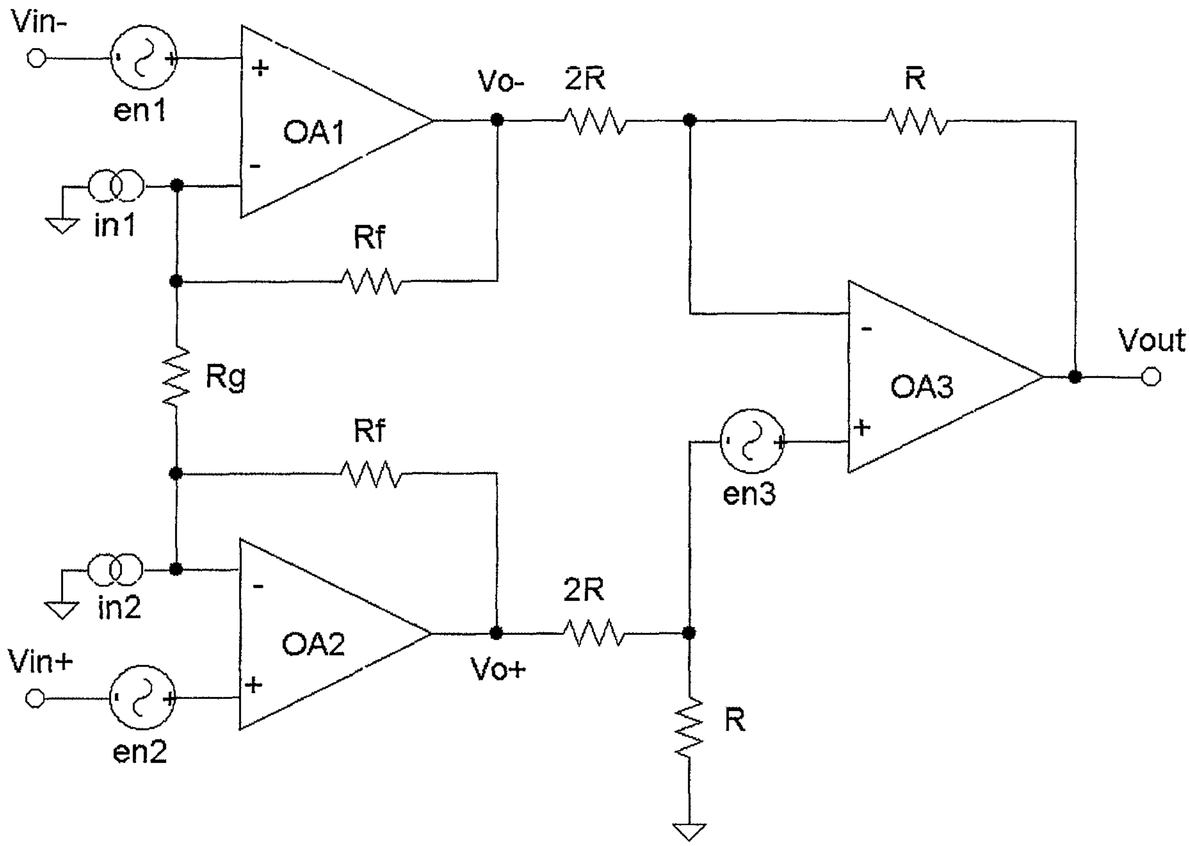

Figure 7. New microphone preamplifier gain scheme.

Substituting (1) and (10) into (9), the noise contribution of the front end gain resistors is as follows:

$$\left[4 \cdot k \cdot T \cdot \frac{Rf}{G}\right] \cdot G^2 \cdot 2 = [4 \cdot k \cdot T \cdot Rf \cdot G] \cdot 2 \qquad (11)$$

The inverting inputs of OA1 and OA2 are virtual grounds. The current noise injected in the inverting input node flows only through feedback resistor Rf. Feedback resistor Rf does the current to voltage conversion and the current noise appears as a voltage at the output of OA1 and OA2. The current noise at the inverting input node comes from multiple sources, such as, the noise of current source into the emitter of the input transistor (refer to Figure 5), the input transistor base current noise. The contribution of current noise sources is as follows:

$$(i_n \cdot Rf)^2 \cdot 2 \qquad (12)$$

The multplication by two comes from the fact that the two current noise sources are not correlated. The difference amplifier gain does not show up in the equation because it is unity.

Noise contribution of operational amplifier OA3 is as follows:

$$e_{n3}^2 \cdot \left(1 + \frac{R}{R}\right)^2 = e_{n3}^2 \cdot 2^2 \qquad (13)$$

The equivalent input noise of the operational amplifier OA3 shows up at the output multiplied by the noise gain of the difference amplifier Although the gain of difference amplifier is unity, the noise gain is two in this case. The noise gain is defined as the gain from the non inverting input of the difference amplifier.

Finally, the noise contribution of the resistor network around the difference amplifier is calculated as follows.

$$\left[\left(4 \cdot k \cdot T \cdot \frac{R}{2}\right) \cdot \left(1 + \frac{R}{R}\right)^2\right] \cdot 2 = \left[\left(4 \cdot k \cdot T \cdot \frac{R}{2}\right) \cdot 2^2\right] \cdot 2 \qquad (14)$$

There are two sets of resistors that are connected to the inputs of OA3. In each set the equivalent resistor value is two resistors of R value in parallel. Since they are equal, the equivalent value is half of R. The thermal noise of the resistors is amplified by the noise gain of the difference amplifier, two in this case. The final multiplication by two is due to the fact that there are two sets of resistors that generate noise and they are not correlated to each other.

The total output noise of the traditional microphone preamplifier can be calculated by adding the noise contributions in (8), (11), (12), (13) and (14).

$$e_n^2 = 2 \cdot e_{n1}^2 \cdot G^2 + 2 \cdot 4kT \cdot Rf \cdot G + 2 \cdot (i_n \cdot Rf)^2 + \\ + 4 \cdot e_{n3}^2 + 8 \cdot 4kT \cdot \frac{R}{2} \tag{15}$$

At low gains each term of the above equation is of the same order of magnitude. At high gains, such as G = 1000, the first term dominates all others. That's why at high gains the noise performance of the front end operational amplifiers OA1 and OA2 is critical. At low gains, the contribution of all other sources of noise becomes dominant.

A similar noise analysis can be done for the new microphone preamplifier architecture shown in Figure 7.

Voltage noise generated by OA1 and OA2:

$$\left\{\left[e_{n1}^2 \cdot \left(1 + \frac{2 \cdot Rf}{Rg}\right)^2\right] \cdot 2\right\} \cdot \left(\frac{1}{2}\right)^2 \tag{16}$$

The equivalent noise of OA1 or OA2 is multiplied by the gain of the amplifier as in the previous case. However, the difference amplifier has a gain of half which multiplies the entire term. Equation (16) can be rearranged and by substituting the gain equation for the new topology (6) into (16) the noise term is calculated as follows:

$$\left[e_{n1}^2 \cdot \left(\frac{1}{2} + \frac{Rf}{Rg}\right)^2\right] \cdot 2 = \left[e_{n1}^2 \cdot G_{new}^2\right] \cdot 2 \tag{17}$$

Similarly, the noise contribution of the front end gain resistors is calculated as follows.

$$\left\{\left[4 \cdot k \cdot T \cdot \left(Rf \| \frac{Rg}{2}\right)\right] \cdot \left(1 + \frac{2 \cdot Rf}{Rg}\right)^2 \cdot 2\right\} \cdot \left(\frac{1}{2}\right)^2 \tag{18}$$

Rearranging the terms in equation (18) and substituting the gain equation (6) into (18), the noise contribution of the front end gain resistors is as follows

$$\left[4 \cdot k \cdot T \cdot \frac{Rf \cdot G_{new}}{2}\right] \cdot 2 \tag{19}$$

Noise contribution of the current noise sources:

$$\left[(i_n \cdot Rf)^2 \cdot 2\right] \cdot \left(\frac{1}{2}\right)^2 \tag{20}$$

Noise contribution of operational amplifier OA3:

$$e_{n3}^2 \cdot \left(1 + \frac{R}{2 \cdot R}\right)^2 = e_{n3}^2 \cdot \left(\frac{3}{2}\right)^2 \tag{21}$$

The noise gain of the new microphone preamplifier topology, as shown in Figure 7, is one and a half. Thus, the equivalent input noise of OA3 is multiplied by that amount.

Finally, the noise contribution of the resistor network around the difference amplifier is calculated as follows:

$$\left[\left(4 \cdot k \cdot T \cdot \frac{2 \cdot R}{3}\right) \cdot \left(1 + \frac{R}{2 \cdot R}\right)^2\right] \cdot 2 \\ = \left[\left(4 \cdot k \cdot T \cdot \frac{2 \cdot R}{3}\right) \cdot \left(\frac{3}{2}\right)^2\right] \cdot 2 \tag{22}$$

The equivalent impedance of each set of resistors connected to the inputs of OA3 is two thirds of resistor value R. This is calculated by paralleling a resistor of value 2 R and a resistor of value R.

The total output noise of the new microphone preamplifier architecture can be calculated by adding the noise contributions in (17), (19), (20), (21) and (22) as follows:

$$e_{n-new}^2 = 2 \cdot e_{n1}^2 \cdot G_{new}^2 + 2 \cdot 4kT \cdot \frac{Rf \cdot G_{new}}{2} + \\ + 2 \cdot \left(i_n \cdot \frac{Rf}{2}\right)^2 + 2.25 \cdot e_{n3}^2 + 4.5 \cdot 4kT \cdot \frac{R}{1.5} \tag{23}$$

Comparing the total noise, at the output of the microphone preamplifier, of the traditional topology, equation (15), to the new architecture, equation (23), it is easy to determine that the latter has lower noise overall. At low gains, all terms are pretty much the same order of magnitude. Therefore, all of them count in the total output noise. At high gains, such as 60 dB (1000), the first term, that contains the noise of the front end operational amplifiers, becomes dominant. This is the reason why the input operational amplifiers need to be very low noise. The second term is the noise of the front end feedback resistor. In the new topology, the feedback resistor appears to be half the value. The third term is the current noise of front end operational

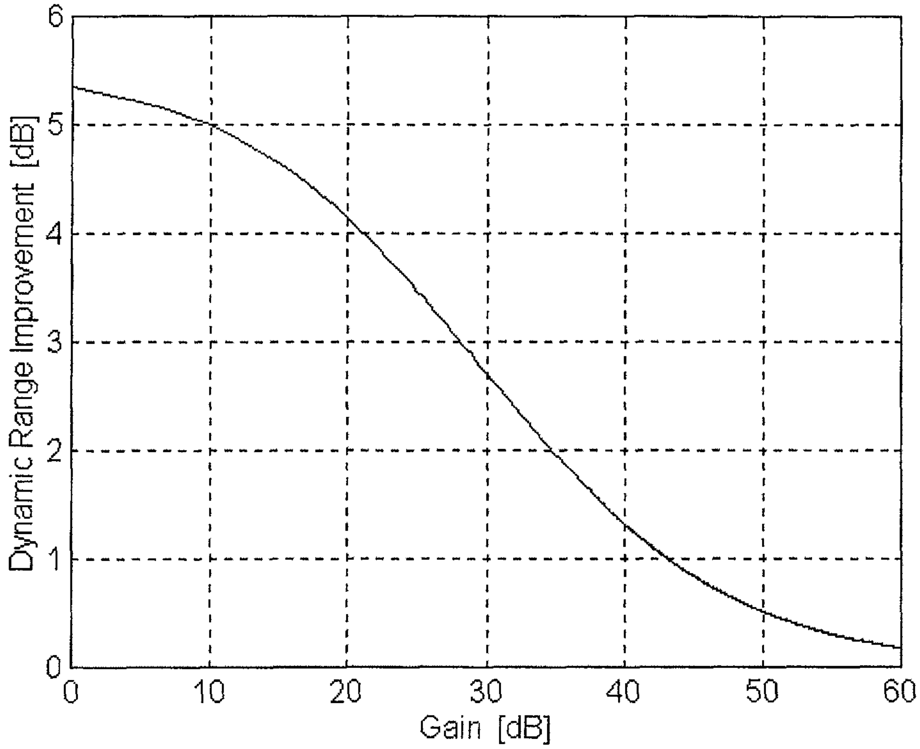

Figure 8. Dynamic range improvement of an existing microphone preamplifier design.

amplifiers, OA1 and OA2, which is two times lower in the new scheme. The fourth term is the noise contribution of the operational amplifier OA3 used in the difference amplifier In the new architecture, this term is about 1.3 times smaller. And finally, the fifth term is the noise of the resistor network in the difference amplifier that is about 1 3 times lower in the new topology

The dynamic range improvement in dB can be expressed as the logarithmic ratio of the noise equation (15) and equation (23) as follows:

$$\Delta DR = 20 \cdot \log \sqrt{\frac{e_n^2}{e_{n-new}^2}} \tag{24}$$

In equation (24), at high gains, the fraction under the square root sign gets closer to unity. Knowing that the logarithm of one is zero, that means that the dynamic range improvement is getting closer to zero when the gain is going up At low gains the noise contribution of the difference amplifier, gain resistors and front end current noise overwhelms the front end voltage noise Also, note that the fraction nominator under the square root sign is always greater than the denominator.

Figure 8 shows a plot of dynamic range improvement versus gain, equation (24), for a microphone preamplifier that has been modified with the new gain scheme. For this example, it was assumed that the voltage noise of the front end amplifier is 1 nV/√Hz, the current noise of the front end operational amplifier is 7 pA/√Hz, the voltage noise of the operational amplifier in the difference amplifier is 6 nV/√Hz and resistors Rf and R are equal to 5 kΩ . As expected, the benefit of the new topology appears at low gains up to about 40 dB

The noise performance of the new microphone preamplifier is improved over older designs especially at low gains Reduced equivalent current noise, i_n , at the inverting input of the front end operational amplifier, lower difference amplifier voltage noise, e_{n3}, combined with the new gain scheme gives a dynamic range advantage of more than 10 dB at lower gains. Figure 9 shows such a plot comparing older designs [2] with the new microphone preamplifier

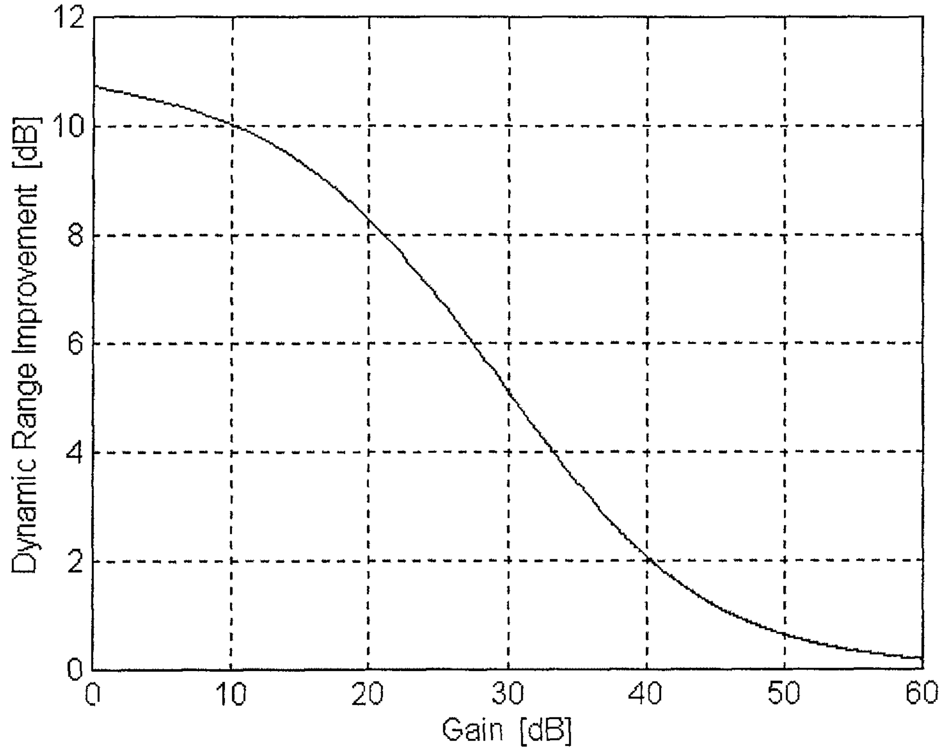

Figure 9. Dynamic range improvement over older designs.

3 CONCLUSION

The details of what makes a good integrated circuit microphone preamplifier were explained throughout the paper It was shown the importance of the semiconductor process on the performance of the preamplifier. Newer semiconductor processes, such as, dielectric isolated complementary bipolar have an edge over older traditional junction isolated process in terms of dynamic range, bandwidth and distortion A microphone preamplifier integrated circuit based on a new architecture is implemented in the dielectric isolated semiconductor process. It improves the dynamic range even further by lowering the noise floor. The idea for the new microphone preamplifier, presented in this paper, has been implemented discretely by a major mixing console manufacturer [11] The new integrated circuit helps in reducing the size of the printed circuit board, eliminate a number of components and finally ıeducing the manufacturing costs.

4 ACKNOWLEDGMENT

The author would like to express his gratitude to Les Tyler for encouraging this paper and Gary Hebert for the valuable suggestions and support.

5 REFERENCES

[1] THAT 1510, "Low Noise, High Performance Microphone," Preliminary Data Sheet, *THAT Corporation*

[2] SSM 2017, "Self-Contained Audio Preamplifier," Data Sheet, Rev. C, *Analog Devices*

[3] INA 103, "Low Noise, Low Distortion Instrumentation Amplifier," Data Sheet, PDS-1016H, *Texas Instruments*

[4] CS5396/97, "120dB, 96kHz Audio A/D Converter,", Data Sheet, M0081-E-00, *Cirrus Logic Incorporated*

[5] AK4394, "Advanced Multi-Bit 192kHz 24bit ΣΔ DAC," Data Sheet, DS229PP2, *Asahi Kasei Microsystems Co , Ltd*

[6] SSM 2018T, "Trimless Voltage Controlled Amplifier," Design-In Reference Manual 1994, *Analog Devices*

[7] THAT 2180, " Pre-Trimmed IC Voltage Controlled Amplifier," Data Sheet, Rev 06/24/99, *THAT Corporation.*

[8] THAT 2252, "IC RMS-Level Detector," Data Sheet, Rev 06/24/99, *THAT Corporation.*

[9] Paul R. Gray and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits, Third Edition," *John Wiley & Sons, Inc.*, pp 149, 1993

[10] Adel S. Sedra, Kenneth C. Smith, "Microelectronic Circuits, Fourth Edition," *Oxford University Press,* pp133, 1998.

[11] VLZ PRO Series Mixing Consoles, Data Sheet, *Mackie Designs Incorporated*